



IEEE GREECE CASS/SSCS  
JOINT CHAPTER

## Invited Lectures

The IEEE Greece CAS/SSC joint Chapter, in the frame of the IEEE Circuits and System Society **Distinguished Lecturer Program**, is inviting you in the lectures of:

**Dr. Rajiv Joshi \***

Researcher at T. J. Watson research centre, IBM, NY,

entitled:

**“Technology Circuit Co-Design  
for Sub-nm Low Power Design”**

The two lectures (joint events) will be given in:

**1) University of Patras on Tuesday, December 6, 2016, at: 13:00, in the Science and Technology Museum.**

*Information:* Prof. Thanos Skodras, tel. 2610-996167, [skodras@upatras.gr](mailto:skodras@upatras.gr)  
Prof. George Alexiou, tel. 2610-996-932, [alexiou@ceid.upatras.gr](mailto:alexiou@ceid.upatras.gr)

**2) Aristotle University of Thessaloniki on Thursday, December 8, 2016, at: 11:00, in the Amphitheater II of KEDEA.**

*Information:* Prof. Alkis Hatzopoulos, tel. 2310-996305, 2310-996221, [alkis@eng.auth.gr](mailto:alkis@eng.auth.gr)

*(There will be live webcasting and recording of the event on December 8, at the link:  
<http://www.auth.gr/video/22952>)*

\* Abstract and lecturer's short bio are following.

# “Technology Circuit Co-Design for Sub-nm Low Power Design”

by

**Dr. Rajiv Joshi**

researcher at T. J. Watson research centre, IBM

**Abstract:** Power has become the key driving force in processor design as the frequency scale-up is reaching saturation. In order to achieve low power system circuit and technology co-design is essential. This talk focuses on related technology and important circuit techniques for nanoscale VLSI circuits. Achieving low power and high performance simultaneously is always difficult. Technology has seen major shifts from bulk to SOI and then to non-planar devices such as FinFET and Trigate.

This talk consists of pros and cons analysis on technology from power perspective and various techniques to exploit lower power. As the technology pushes towards sub-22nm era, process variability and geometric variation in devices can cause variation in power. The reliability also plays an important role in the power-performance envelope. This talk also reviews the methodology to capture such effects and describes all the power components. All the key areas of low power optimization such as reduction in active power, leakage power, short circuit power and collision power are covered. Usage of clock gating, power gating, longer channel, multi-Vt design, stacking, header-footer device techniques and other methods are described for logic and memory. Finally the talk summarizes key challenges in achieving low power.

**Dr. Rajiv V. Joshi** is a research staff member at T. J. Watson research center, IBM. He received his B. Tech I.I.T (Bombay, India), M.S (M.I.T) and Dr. Eng. Sc. (Columbia University). His novel interconnects processes and structures for aluminum, tungsten and copper technologies which are widely used in IBM for various technologies from sub-0.5 $\mu$ m to 14nm. He has led successfully pervasive statistical methodology for yield prediction and also the technology-driven SRAM at IBM Server Group. He commercialized these techniques. He received 3 Outstanding Technical Achievement (OTAs), 3 highest Corporate Patent Portfolio awards for licensing contributions, holds 57 invention plateaus and has over 215 US patents and over 350 including international patents. He has authored and co-authored over 185 papers. He is recipient of 2015 BMM award. He is inducted into New Jersey Inventor Hall of Fame in Aug. 2014 along with pioneer Nikola Tesla. He is a recipient of 2013 IEEE CAS Industrial Pioneer award and 2013 Mehboob Khan Award from Semiconductor Research Corporation. He is a member of IBM Academy of technology. He served as a Distinguished Lecturer for IEEE CAS and EDS society. He is IEEE and ISQED fellow and distinguished alumnus of IIT Bombay. He is in the Board of Governors for IEEE CAS. He serves as an Associate Editor of TVLSI. He served on committees of ISLPED (Int. Symposium Low Power Electronic Design), IEEE VLSI design, IEEE CICC, IEEE Int. SOI conference, ISQED and Advanced Metallization Program committees. He served as a general chair for IEEE ISLPED. He is an industry liaison for universities as a part of the Semiconductor Research Corporation. Also he is in the industry liaison committee for IEEE CAS society.