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Murphy Goes 3D

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Abstract

"Whatever can, will go wrong" is the famous quote attributed to Captain Edward Murphy. It has given Murphy the status of patron saint of all test engineers, since it is Murphy's Law that keeps them in business.

Three-dimensional stacking of ICs have kept the communities in both technology and design research busy for several years now. No wonder, because 3D-SICs hold the promise of heterogeneous integration, inter-die connections with increased performance at lower power dissipation, and increased yield and hence decreased product cost. However, all these benefits can only materialize if 3D-SICs can be properly tested for manufacturing defects. Only recently, the test community has started to work on test solutions for these IC products, signaling that their high-volume market introduction is now imminent.

This talk gives an overview of 3D-SIC technologies, associated test challenges, and emerging solutions.

Biography

Erik Jan Marinissen is Principal Scientist at IMEC vzw in Leuven, Belgium, where he is responsible for the research on test and design-for-test of 3D-stacked ICs. In addition, he is Visiting Researcher at the University of Technology in Eindhoven, the Netherlands. Previously, he worked at NXP Semiconductors and Philips Research, both in Eindhoven. Marinissen holds an MSc degree in Computing Science (1990) and a PDEng degree in Software Technology (1992), both from Eindhoven University of Technology. Marinissen's research interests include all topics in the domain of test and debug of micro-electronics. He is co-author of over 230 journal and conference papers and co-inventor on twelve granted US and EP patent families. Marinissen is recipient of the Most Significant Paper Awards at ITC 2008 and ITC 2010, Best Paper Awards at the Chrysler-Delco-Ford Automotive Electronics Reliability Workshop 1995 and the IEEE International Board Test Workshop 2002, and the Most Inspirational Presentation Award at the IEEE Semiconductor Wafer Test Workshop 2013. He served as Editor-in-Chief of IEEE Std 1500 and is Founder and Chair of the IEEE P1838 Working Group on 3D test access. Marinissen is founder of workshops on 'Diagnostic Services in Network-on-Chips' (DSNOC), '3D Integration', and 'Testing of Three-Dimensional Stacked Integrated Circuits' (3D-TEST). He has been Program Chair of DDECS'02, ETS'06, 3D-TEST'09-'13, and DATE'13, and General Chair of ETW'03, DSNOC'07-'08, 3DIW'09-'10, and continues to serve on numerous conference committees, including ATS, DATE, ETS, ITC, and VTS. He serves on the editorial boards of IEEE Design & Test of Computers, IET Computers and Digital Techniques, and Springer's Journal of Electronic Testing: Theory and Applications (JETTA). Marinissen is a Fellow of IEEE and Golden Core Member of Computer Society.