High Speed Interconnect Design and Characterization

Jay Diepenbrock

April, 2014

IEEE

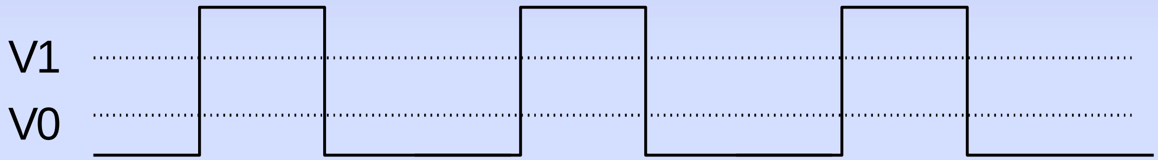
EMC SOCIETY

Outline

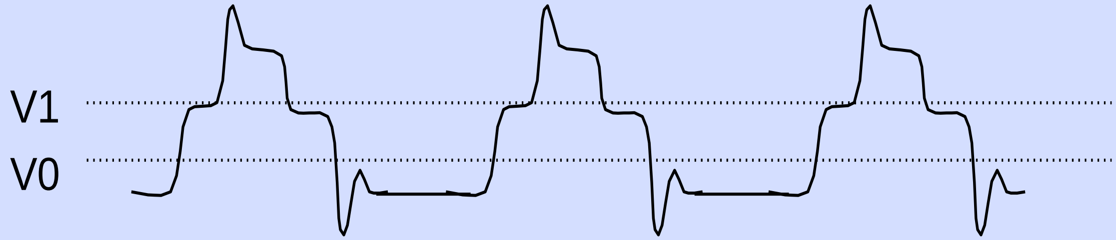
- Signal Integrity - what, why, and how?
- Electrical characteristics of interconnect structures
  - basic properties - determined by materials, dimensions, etc.
  - measurement techniques and tools
- "Real world" component examples
  - capacitors (e. g., decoupling)
  - vias
  - connectors
- Attenuation
  - what is it?
  - what causes it
  - what are its effects?
- Resources and References

What is Signal Integrity?

- Maximizing *probability* of delivering a signal from point A to point B without errors
- Managing signal quality, shape, etc. as seen by receiver circuits
- It's all about rise time, discontinuities, and frequency dependent losses
- Signal speeds, frequencies increasing
- Spatial resolution and frequency spectrum directly related to rise time



Ideal signal
- square edges,
- no noise,
- no interaction

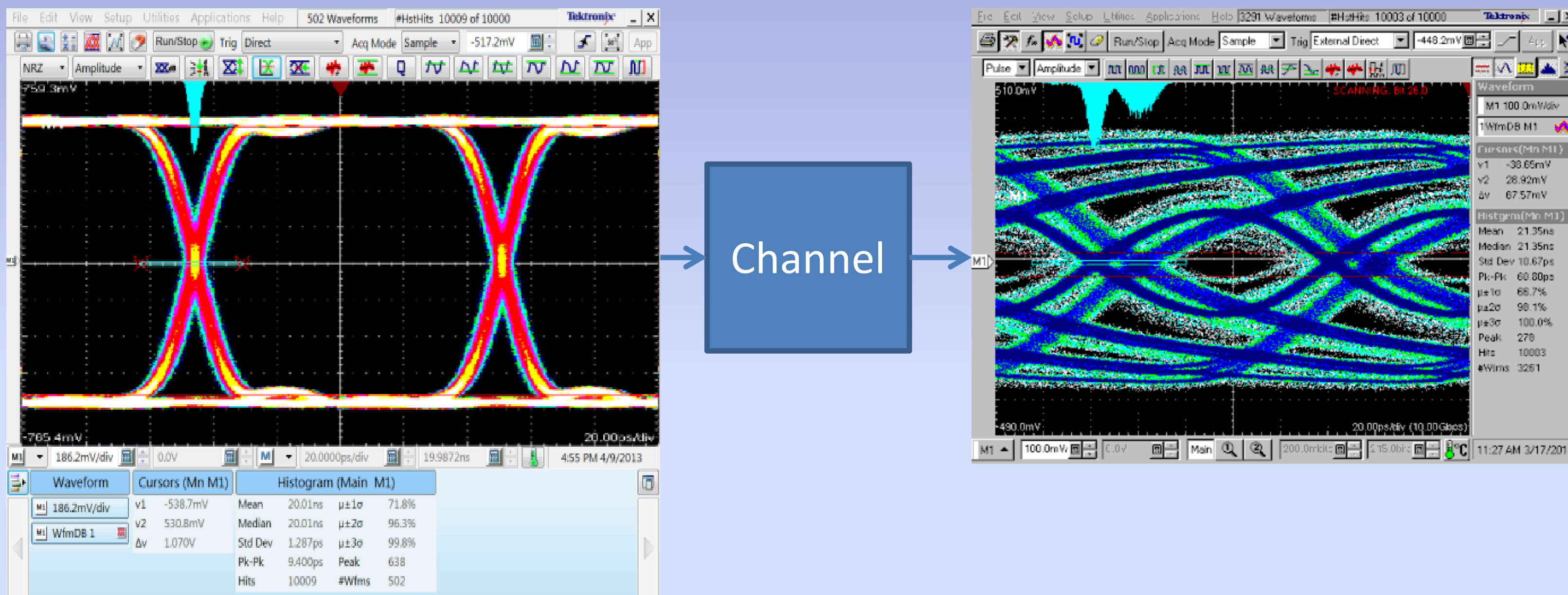


Real signal
- nasty edges,
- noise,
- reflections

Signal Distortion

What goes in

What comes out



- Why?
- What can be done about it?

What is Signal Integrity?

- Multidisciplinary
  - **Analog**
  - Digital Signal Processing
    - Complex signal modulation
    - Equalization
  - Error detection and correction
  - Packaging
  - “Black Magic” fields of
    - Electromagnetics
    - Radio Frequency (RF)
    - Microwaves
    - Transmission Lines
  - Power supplies and distribution
  - Software – layout, analysis
  - Testing

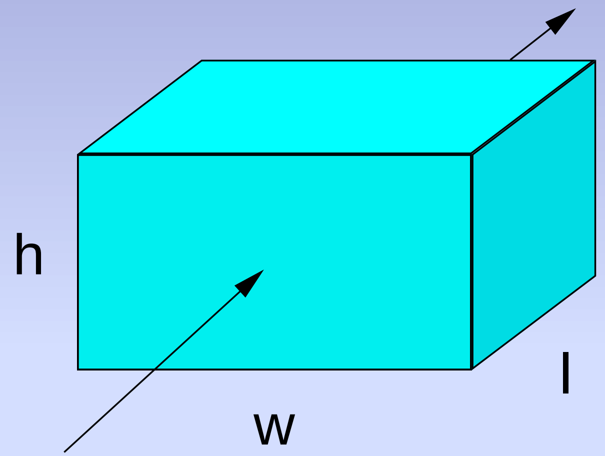
“Digital is just a special case of **analog**” – G. Philbrick, ca. 1950

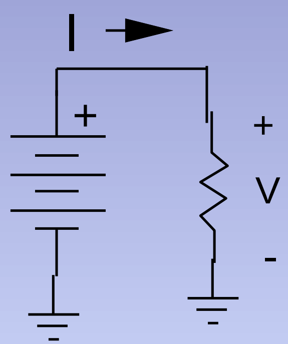
Electrical characteristics of interconnects

- DC
  - resistance
  - opens/shorts
  - HiPot
  - Insulation resistance
- AC, low frequency quantities and measurements
  - capacitance
  - inductance
  - impedance
- AC, high frequency quantities and measurements
  - impedance
  - attenuation
  - crosstalk
  - jitter and eye patterns

DC resistance

causes DC voltage drop, V=I*R





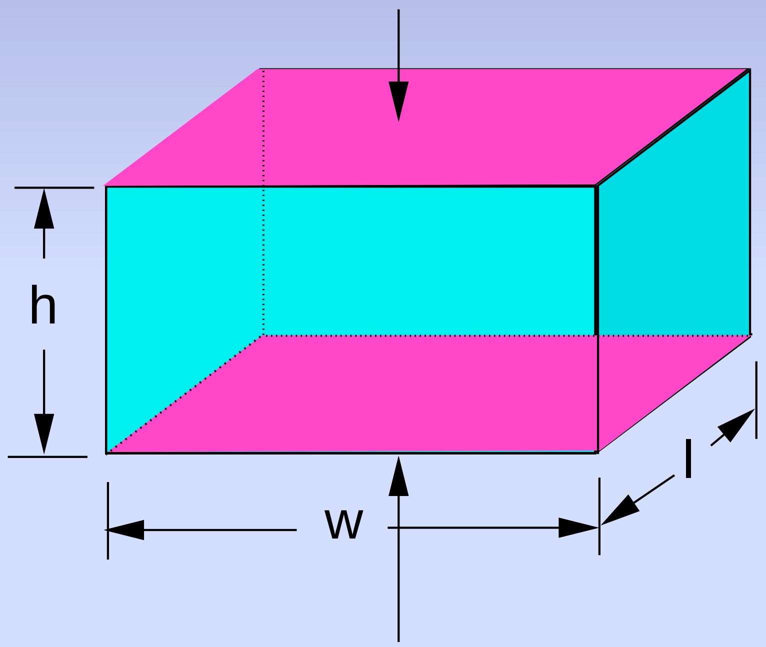
- bulk resistivity =
- ρ Ω-cm or ρ_s Ω/square

$$R = \rho * l/(h*w) = \rho_s * l/w$$

"sheet" resistivity   # squares

Capacitance

stores charge, $Q=V*C$, $V= 1/C\int i\,dt$



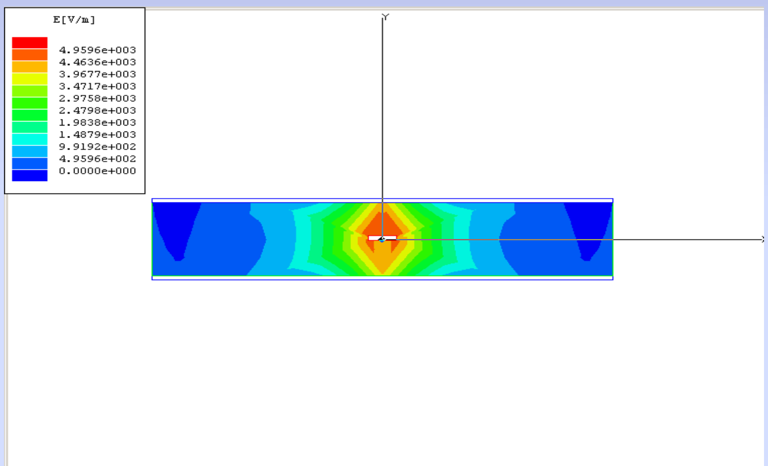
- $C=\varepsilon*l*w/h = \varepsilon*A/h$, where
- A = surface area of plates
- h = plate separation
- $\varepsilon=\varepsilon_r*\varepsilon_0$, with

  ε_r = material relative permittivity and

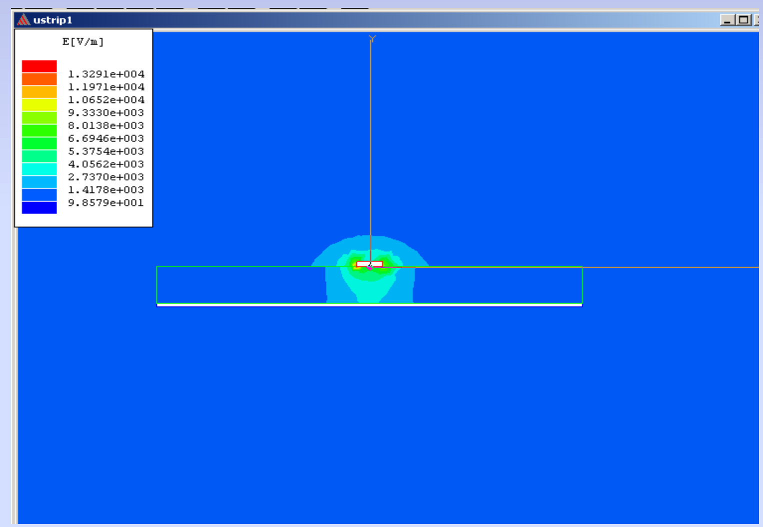
  ε_0 = permittivity of air = 8.854x10-12 F/m
- typical ε_r values:
  - air = 1.0
  - PTFE = 2.0 (lower if expanded)
  - FR-4 = 4.5
- Example:
  - 1x1" FR-4 PCB plate,
  - 10 mil spacing between planes
  - C = 101 pF

Capacitance

- Complications:
  - fringing fields with narrow lines
  - inhomogeneous dielectrics (e. g., microstrip)
  - Temperature, frequency dependence



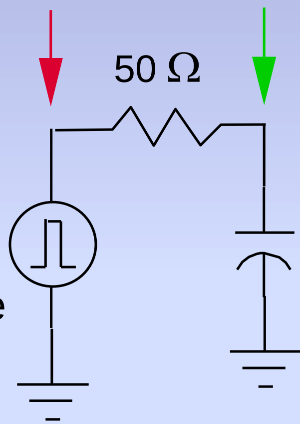
(stripline field plot)

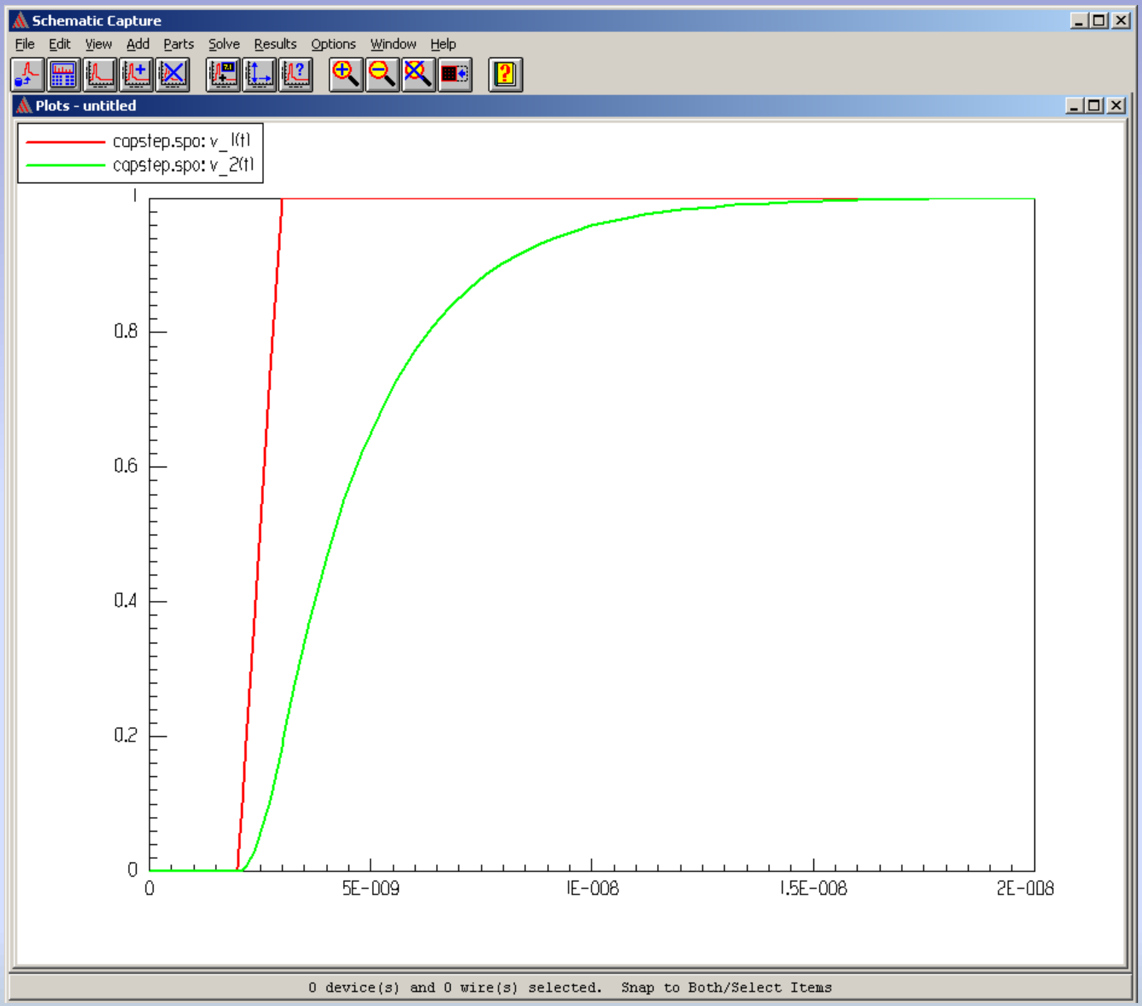


(microstrip field plot)

Measurement: LCR meter, impedance bridge, etc. (must specify freq.)

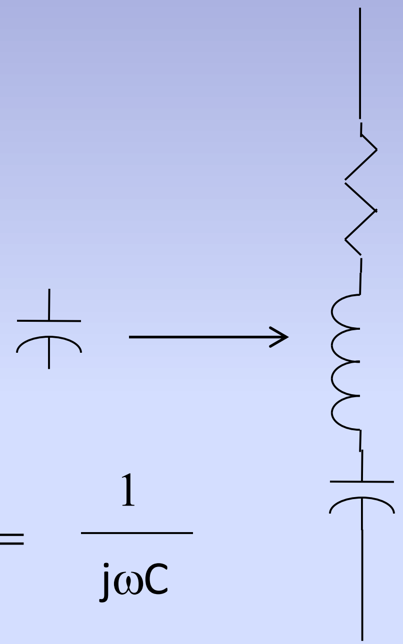
Capacitance



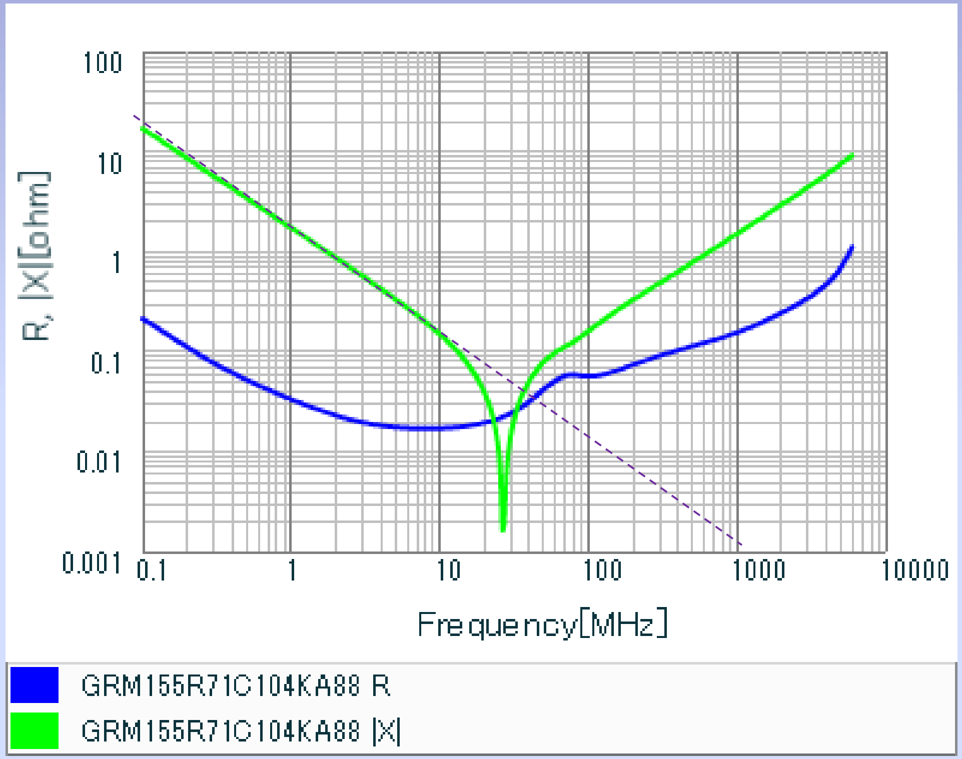


Capacitance – real capacitors

(when is a capacitor not a capacitor?)



$$Z = \frac{1}{j\omega C}$$



Plot courtesy of muRata Erie

$$Z = R + j\omega L + \frac{1}{j\omega C}$$

Dielectric Loss

- Recall, $\gamma = \sqrt{(R + jwL)(G + jwC)} = \alpha + j\beta$

  and attenuation = $20 \log_{10} e^{\mathrm{Re}\,\gamma} = 20 \log_{10} \exp\sqrt{(RG-\omega^2 LC)}$

- Dielectric constant of the medium, $\varepsilon = \varepsilon(1 - j \tan \delta_l)$,

  so $G = \sigma C/\varepsilon = \sigma C/D_k = \omega C \tan \delta = \omega C \tan D_f$

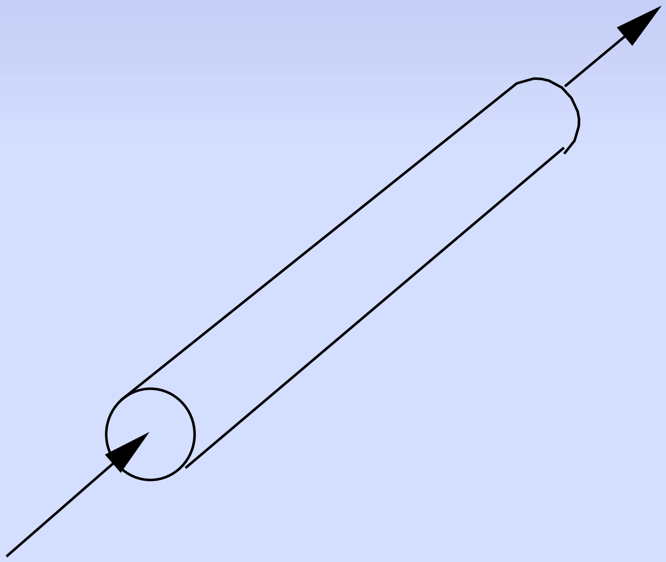
  Increasing frequency -> shunt losses

- Typical values:

Material	ε	$\tan \delta$
FR-4 (normal glass-epoxy card material)	4.5	0.02
NELCO 4000-13	3.7	0.008
Megtron-6	3.5	0.005
PTFE (Teflon)	2.1	0.0003

Inductance

opposes AC current flow, $v = L\, di/dt$



- Internal inductance, $L = \mu/8\pi$ H/m
- where $\mu = \mu_r\mu_0$, with

  μ_r = material relative permeability,

  μ_0 = permeability of free space

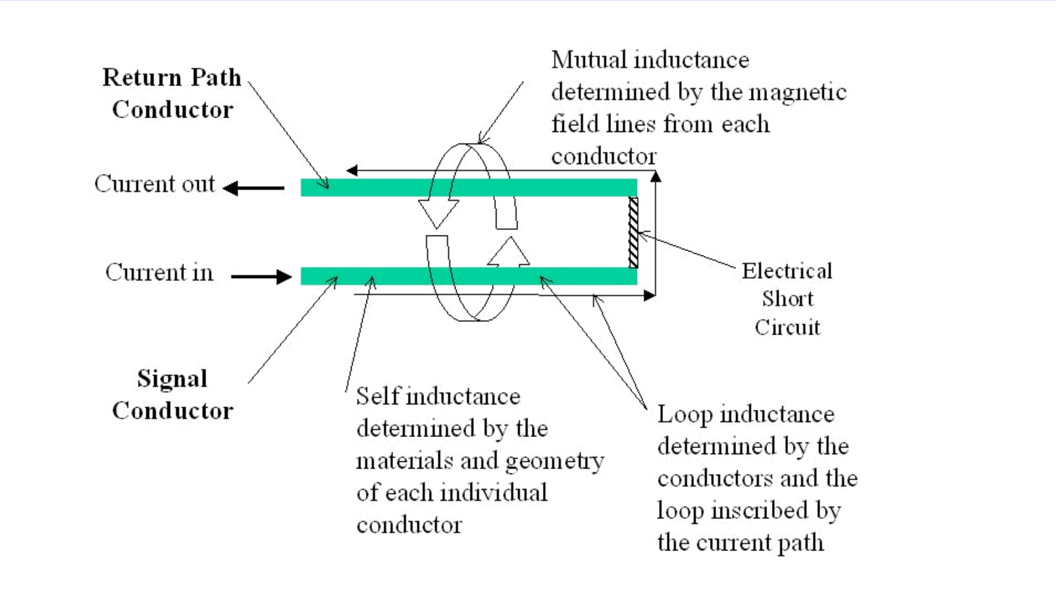
  = 4π x10-7 H/m
- (round, infinitely long straight wire in
- free space w/ uniform current distribution)

Note:

- independent of wire diameter
- free space - no adjacent conductors!

Inductance

- Complications:
  - "Ground"
  - loop inductance vs. self-inductance
  - other adjacent conductors, return path



Measurement: LCR meter, impedance bridge, etc. (must specify freq.)

Inductance - real wires

- L = 0.002 l * [2.3 log10 ((4 l / d) - 0.75)] uH,

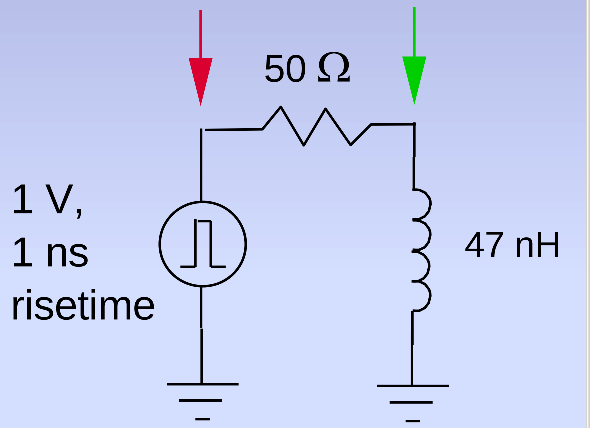
  where l = wire length, cm

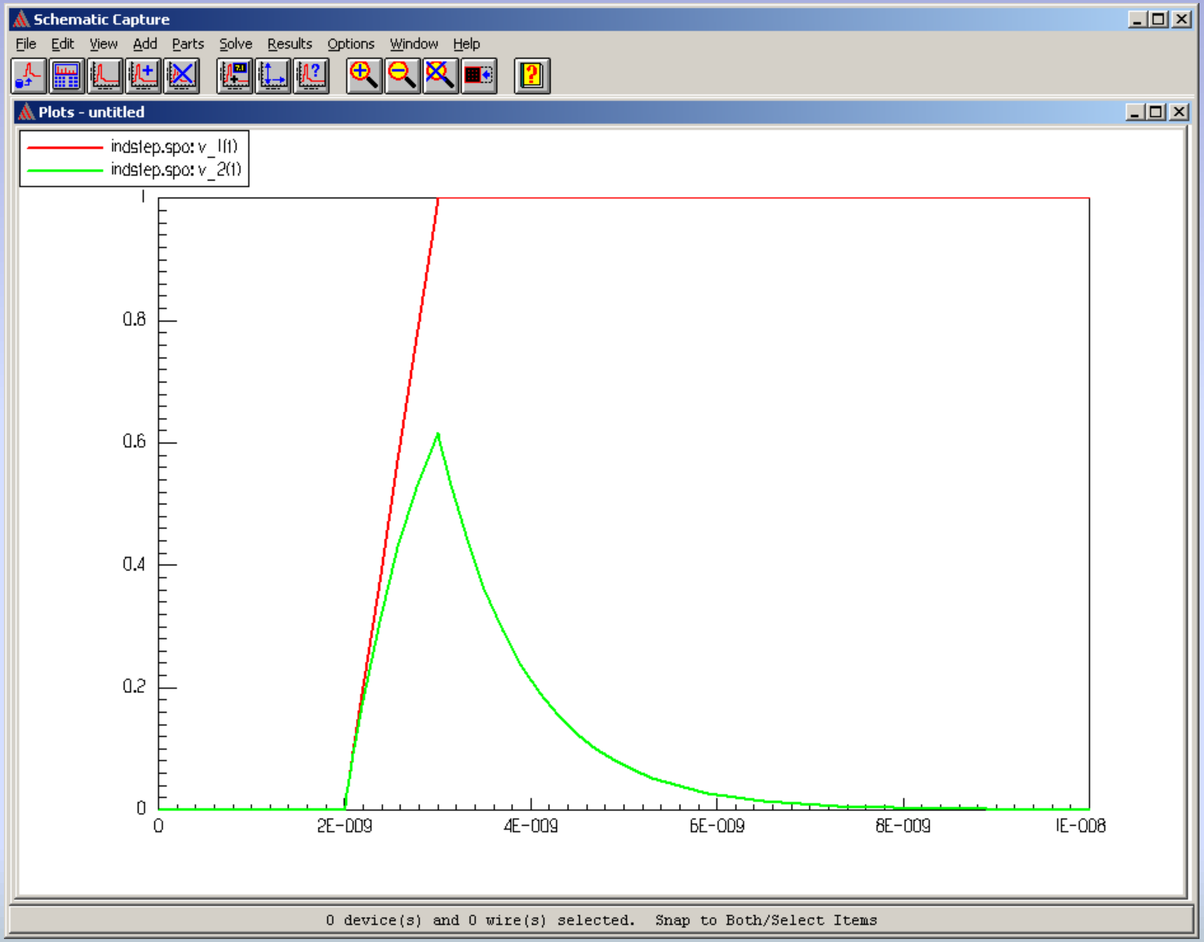
  d = wire diameter, cm

- Typical values:

Wire size, AWG	Diameter, cm	Resistance, mOhms/m	Inductance, nH/cm
20	.0813	3.10	7.8
22	.0642	4.94	8.2
24	.0511	7.83	8.7
26	.0404	12.5	9.2
28	.0320	19.9	9.6
30	.0254	31.7	10.1

Inductance


50 Ω
1 V,
1 ns
risetime
47 nH


Schematic Capture
File Edit View Add Parts Solve Results Options Window Help
Plots - untitled
indstep.spo: v_1(1)
indstep.spo: v_2(1)
1
0.8
0.6
0.4
0.2
0
0
2E-009
4E-009
6E-009
8E-009
1E-008
0 device(s) and 0 wire(s) selected. Snap to Both/Select Items

Impedance

- Causes AC voltage drop, v = i*Z
- Units are Ohms, just like DC resistance
- In simplest form, $Z = (L/C)^{1/2}$, where L and C are per unit length

- You might ask: Why should I care?
- A better question: *When* should I care?

Impedance

- Causes AC voltage drop, v = i*Z
- Units are Ohms, just like DC resistance
- In simplest form, $Z = (L/C)^{1/2}$, where L and C are per unit length

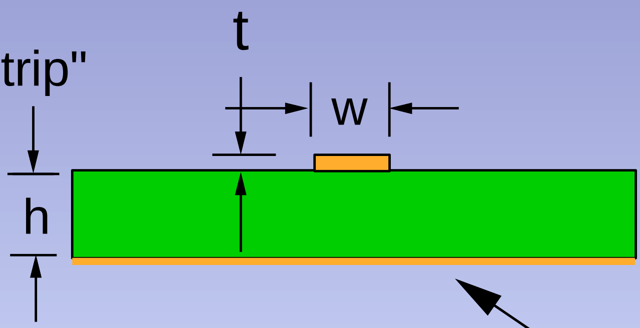
- You might ask: Why should I care?
- A better question: *When* should I care?
- Answer: when electrical length of interconnect segment > ~λ/10, or
  when electrical length of interconnect segment > ~trise/2
  (electrical length = signal propagation delay in medium)
  - Examples
    - card microstrip (surface) wiring t_{prop} ~= 170 ps/in.
    - cable t_{prop} ~= 110 ps/in.

    Note: tprop. ~= $C/(\varepsilon_r)^{1/2}$, C = speed of light *in the medium*

  Note: Each segment has a different impedance (and prop. delay)!
- So, what's the problem? The problem is discontinuities (interfaces)

Card wiring impedance

"Microstrip"

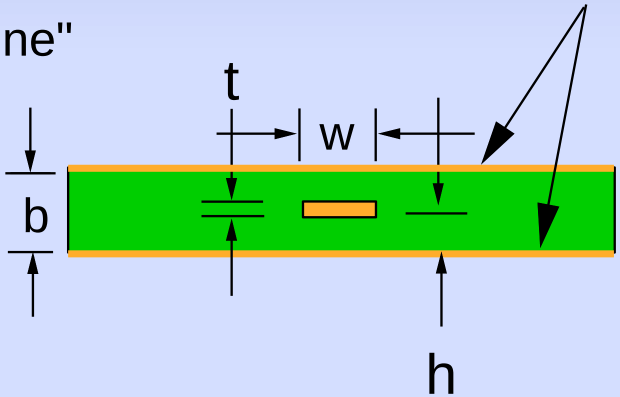


$$Z0 = \frac{87}{\sqrt{\epsilon_r}+1.41} \ln\left(\frac{5.98*h}{0.8w+t}\right)$$

example: w=6, t=1.4, h=12 -> Z0=60 Ω

Ground planes

"Stripline"

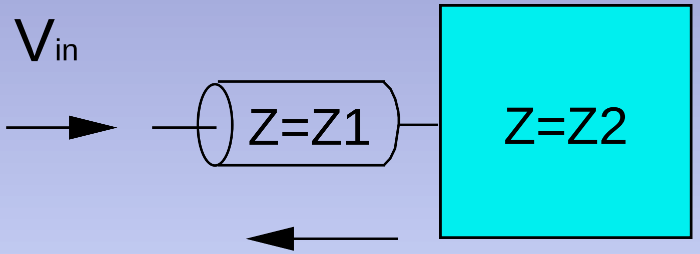


$$Z0 = \frac{60}{\sqrt{\epsilon_r}} \ln\left(\frac{4b}{0.67\pi w\left(0.8+\frac{t}{w}\right)}\right)$$

example: w=6, t=1.4, b=12, h=6 -> Z0=37 Ω

Notes: 1. The stripline may not be vertically symmetric (can be unequal spacing to planes)
2. Other variations exist; e. g., covered microstrip (stripline w/o upper Ground plane)
Reference: Blood: MECL Handbook

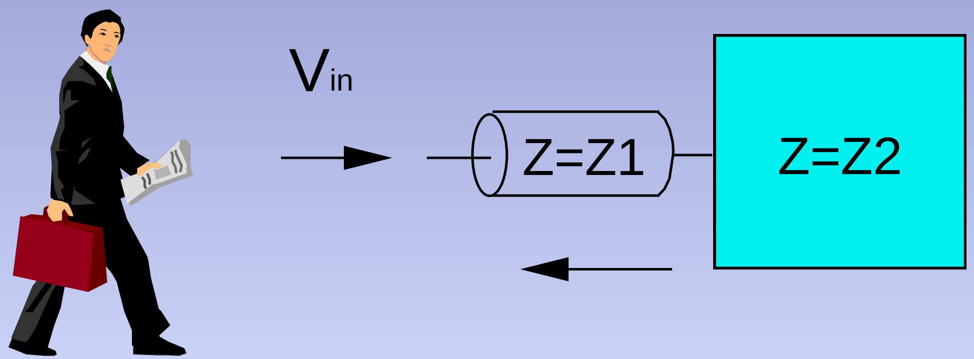
Impedance



Reflection coefficient, $\rho = \frac{V_{refl}}{V_{in}} = \frac{Z2-Z1}{Z2+Z1}$ (can be + or -, and may be called Γ)

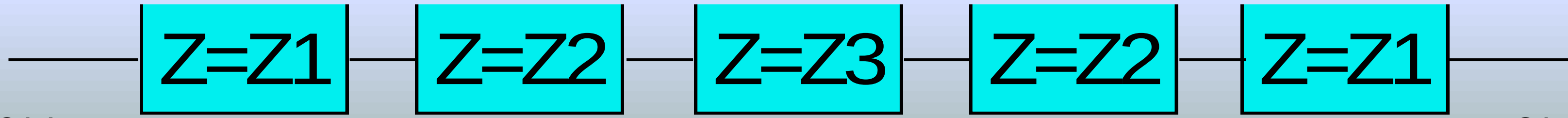
Another useful relationship: $VSWR = \frac{1+\rho}{1-\rho}$

Impedance



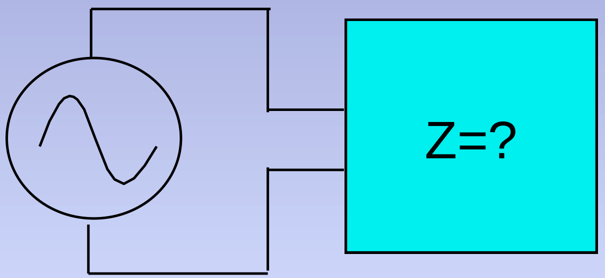
Reflection coefficient, $\rho = \dfrac{V_{refl}}{V_{in}} = \dfrac{Z2-Z1}{Z2+Z1}$ (can be + or -, and may be called Γ)

Imagine what would happen if you had this:



Impedance measurement

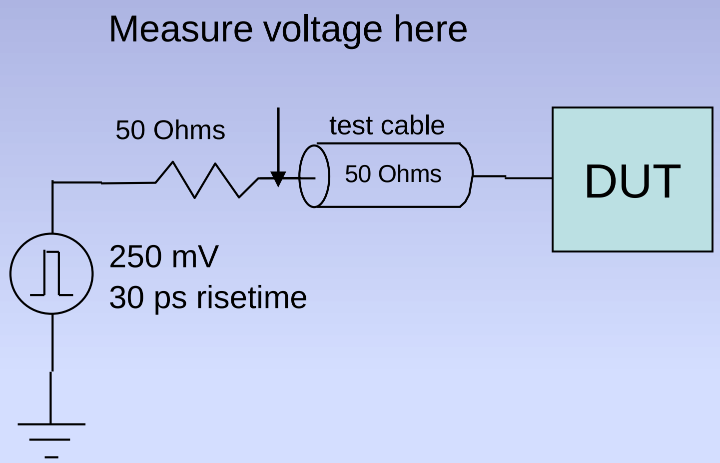
Impedance Bridge



- AC source (oscillator) - must specify frequency (ies)
- Measures R, L, C, Z looking into DUT
- Subject to inaccuracy due to
- resonance of DUT at measurement freq.
- discontinuities in DUT - no position-dependent info

Impedance measurement

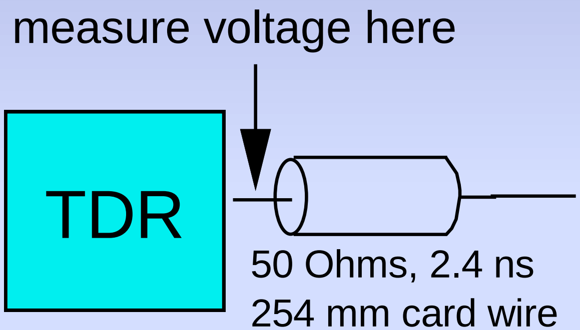
- Time Domain Reflectometer (TDR)



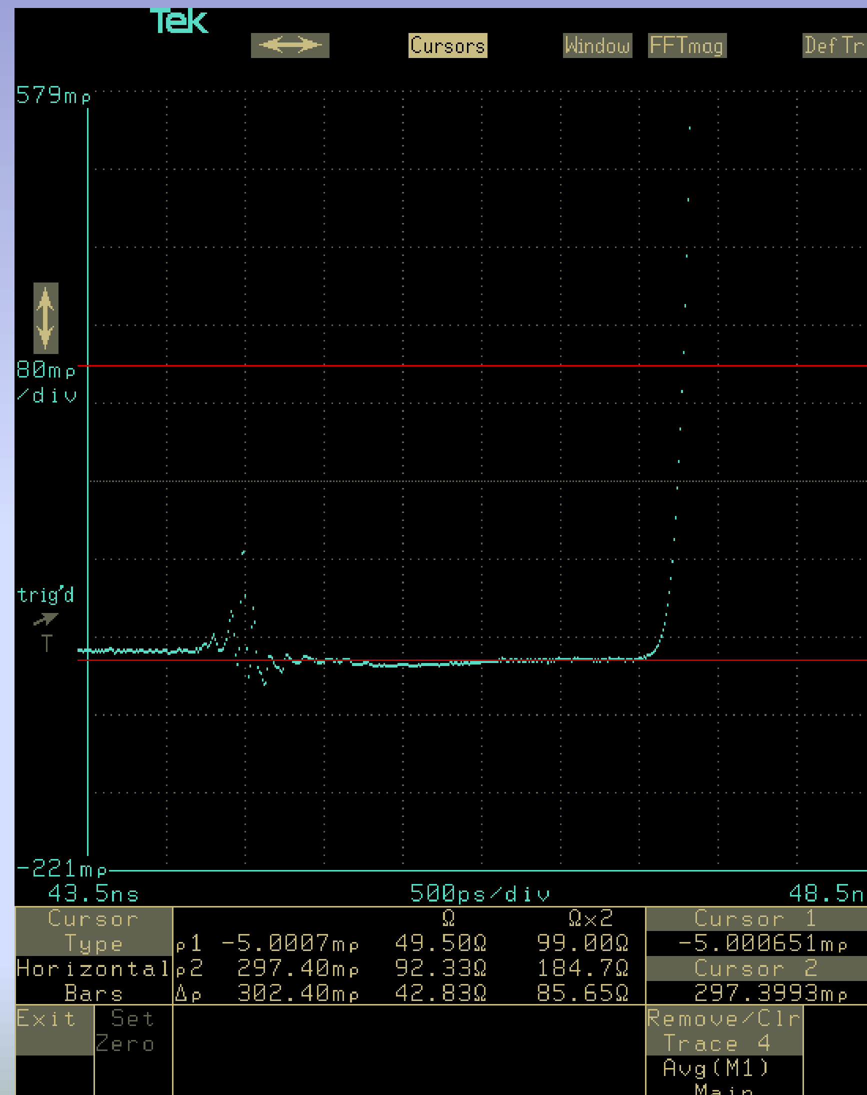
- time domain measurement - measures Z vs. time (distance)
- can be single-ended (shown) or differential (if equipment capable)
- accuracy, resolution degrade with
    - loss in test cables and DUT
    - probe effects (large ground loops, etc.)
- risetime is everything!

Impedance example 1

- Matched line, open circuited end



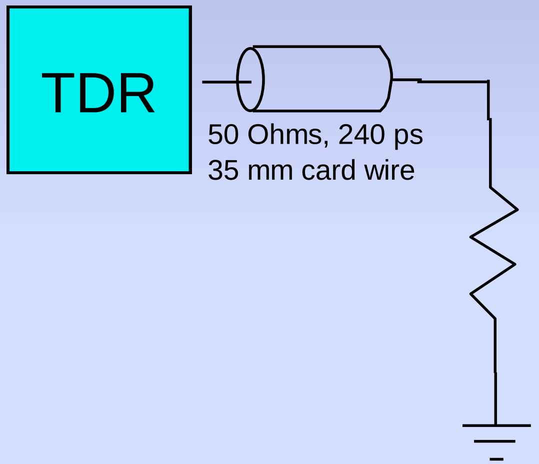
cursors: 1=51.1 Ω
2=N/A

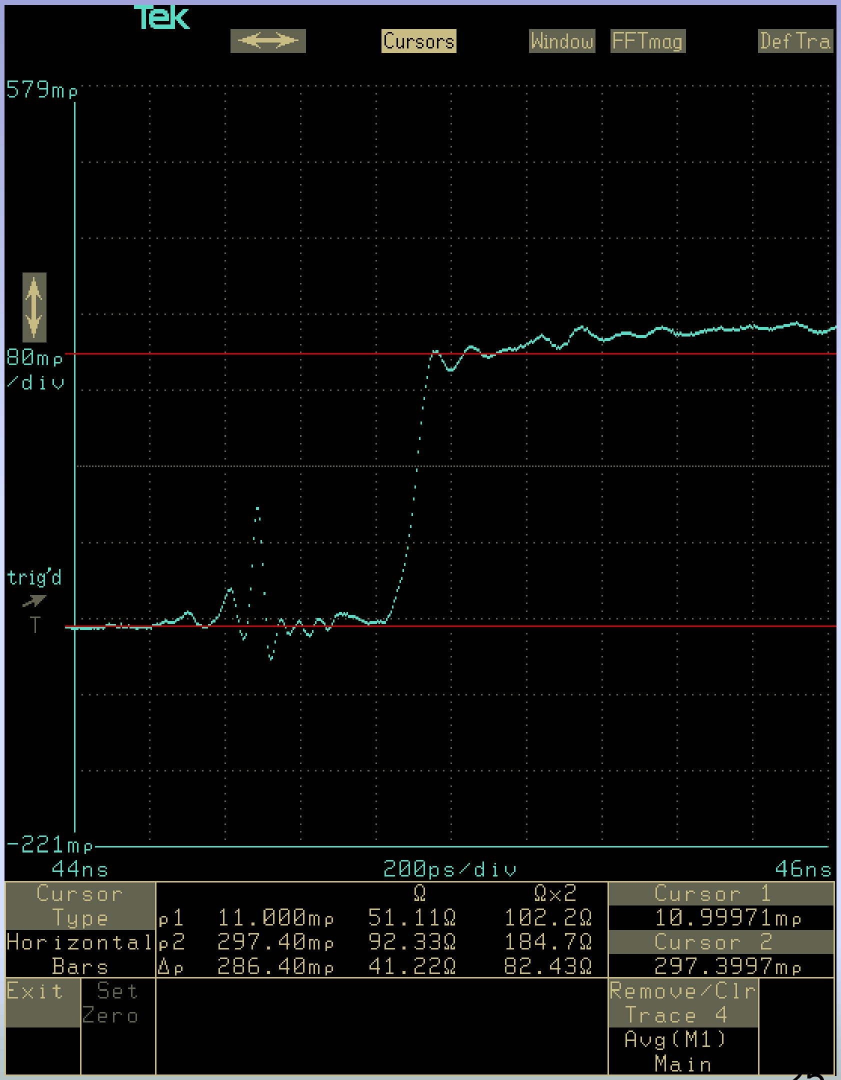


A TDR is a debugger's friend!

Impedance example 2

- Matched line,
  mismatched resistive load

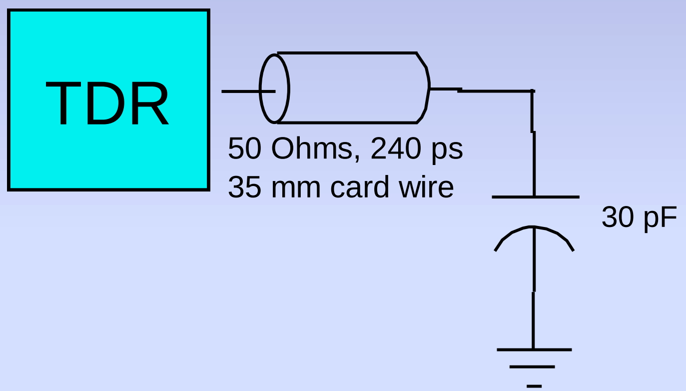


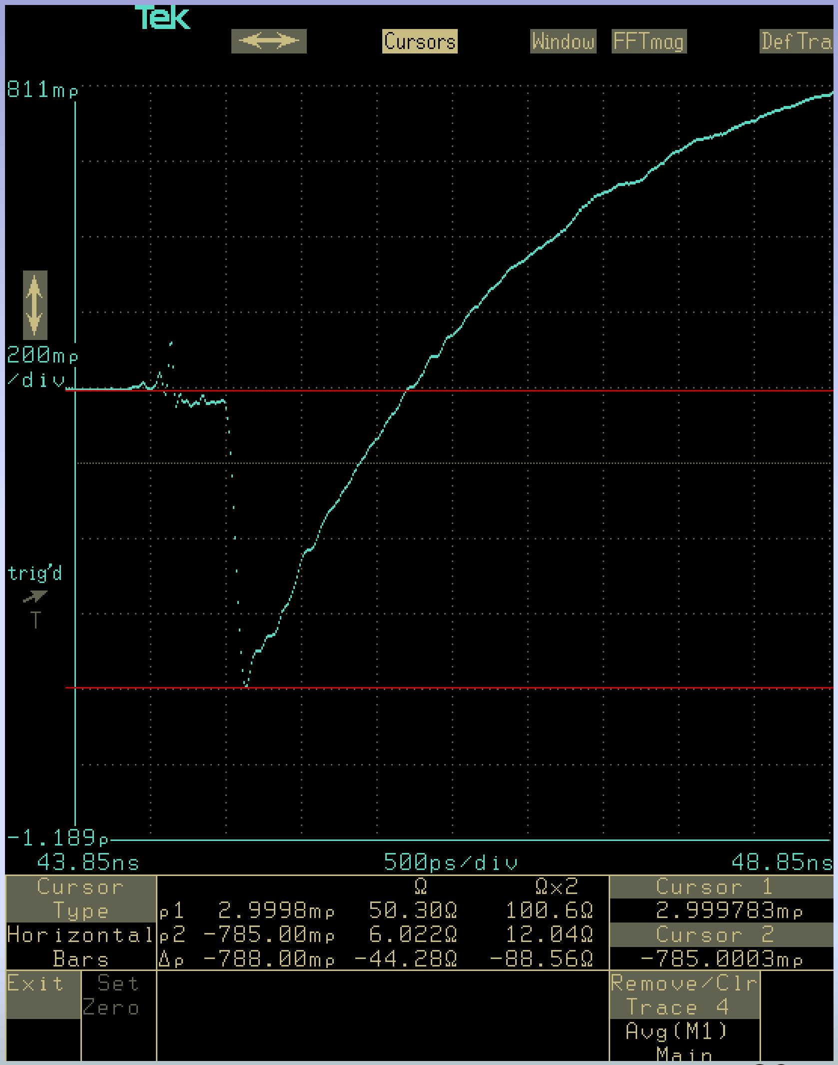


cursors: 1=51.1 Ω
2=92.33 Ω

Impedance example 3

- Matched line, capacitive load



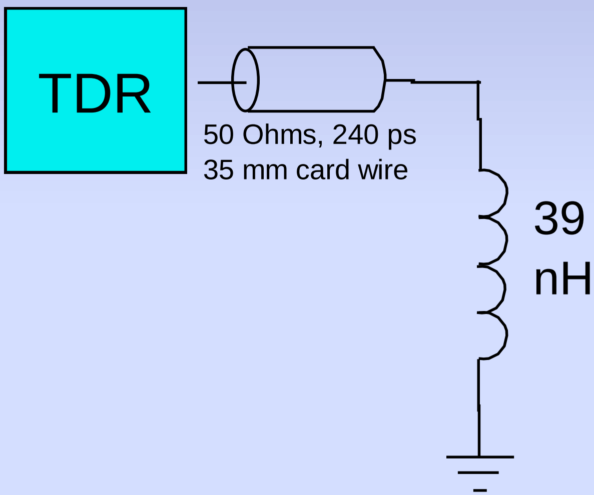


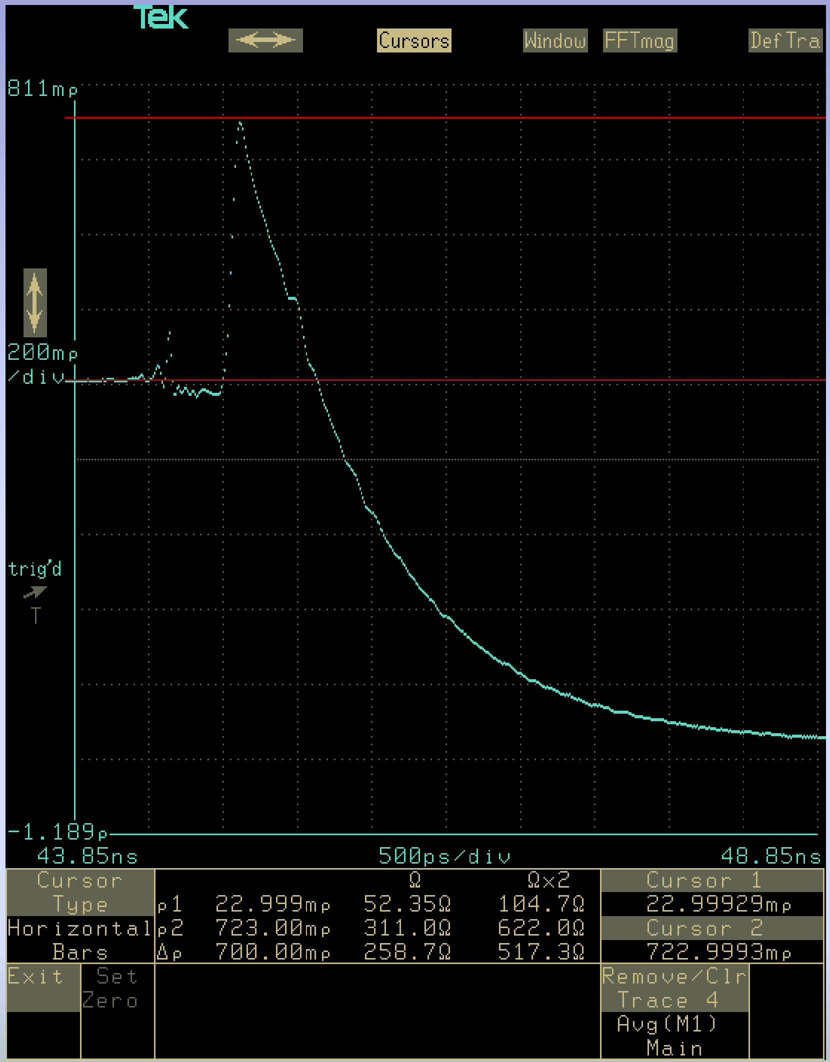
cursors: 1=50.30 Ω

2=6.22 Ω

Impedance example 4

- Matched line, inductive load

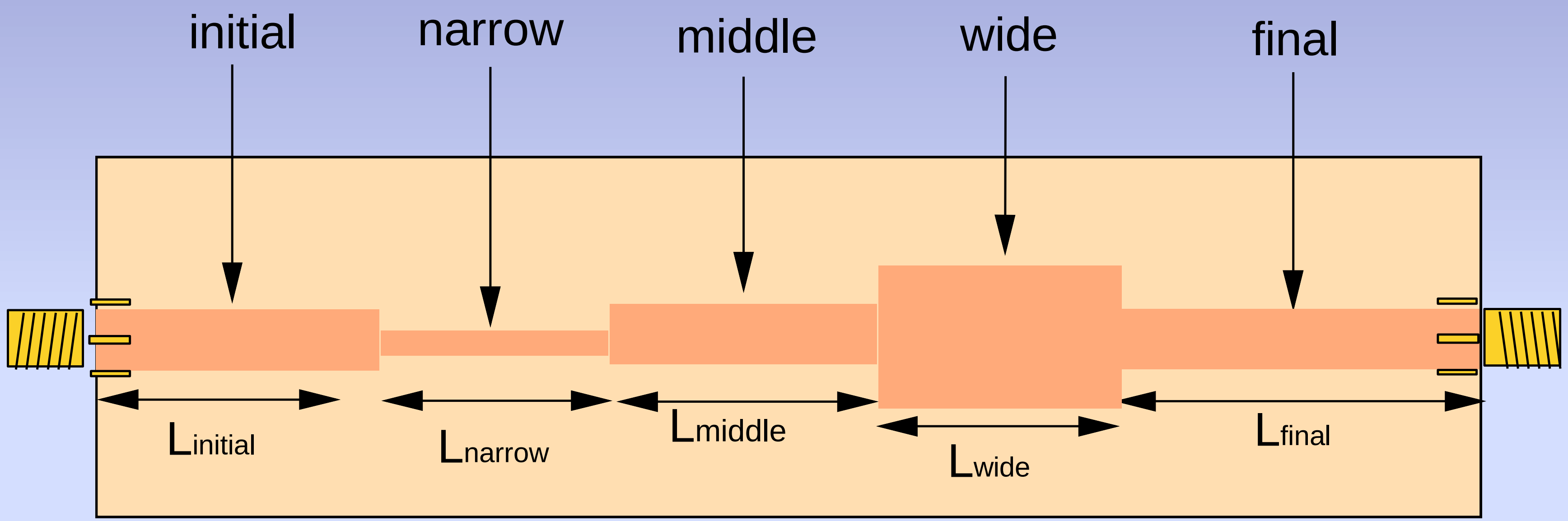




cursors: 1=52.35 Ω
2=311 Ω

Impedance example 5

“ugly” network

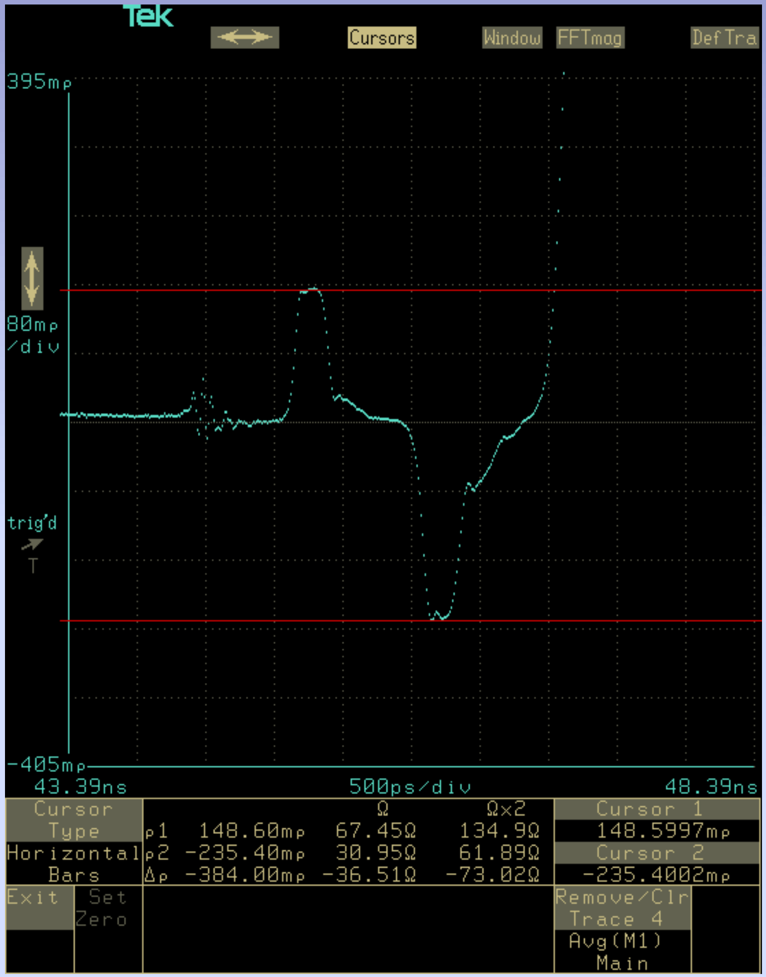


Winitial = 2.77 mm
Wnarrow = 1.24 mm
Wmiddle = Winitial
Wwide = 7.58 mm
Wfinal = Winitial

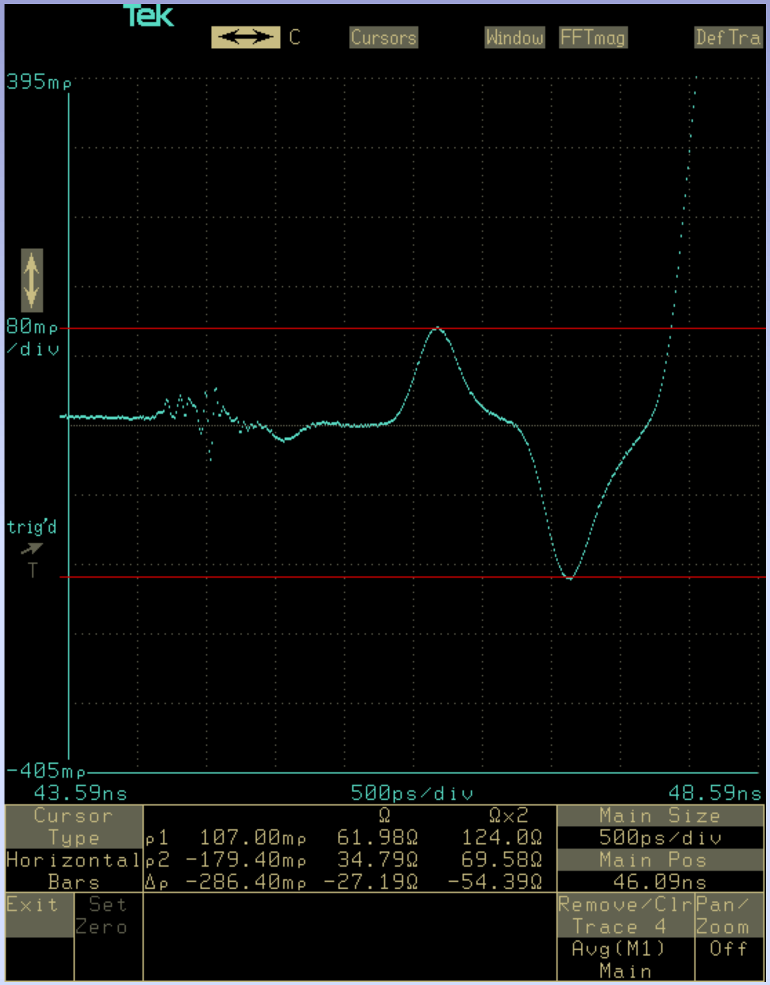
Linitial = 53 mm
Lnarrow = 20 mm
Lmiddle = 56 mm
Lwide = 20 mm
Lfinal = 53 mm

Zinitial = 50 Ω
Znarrow = 67 Ω
Zmiddle = Zinitial
Zwide = 31 Ω
Zfinal = Zinitial

"Ugly" network TDR plots

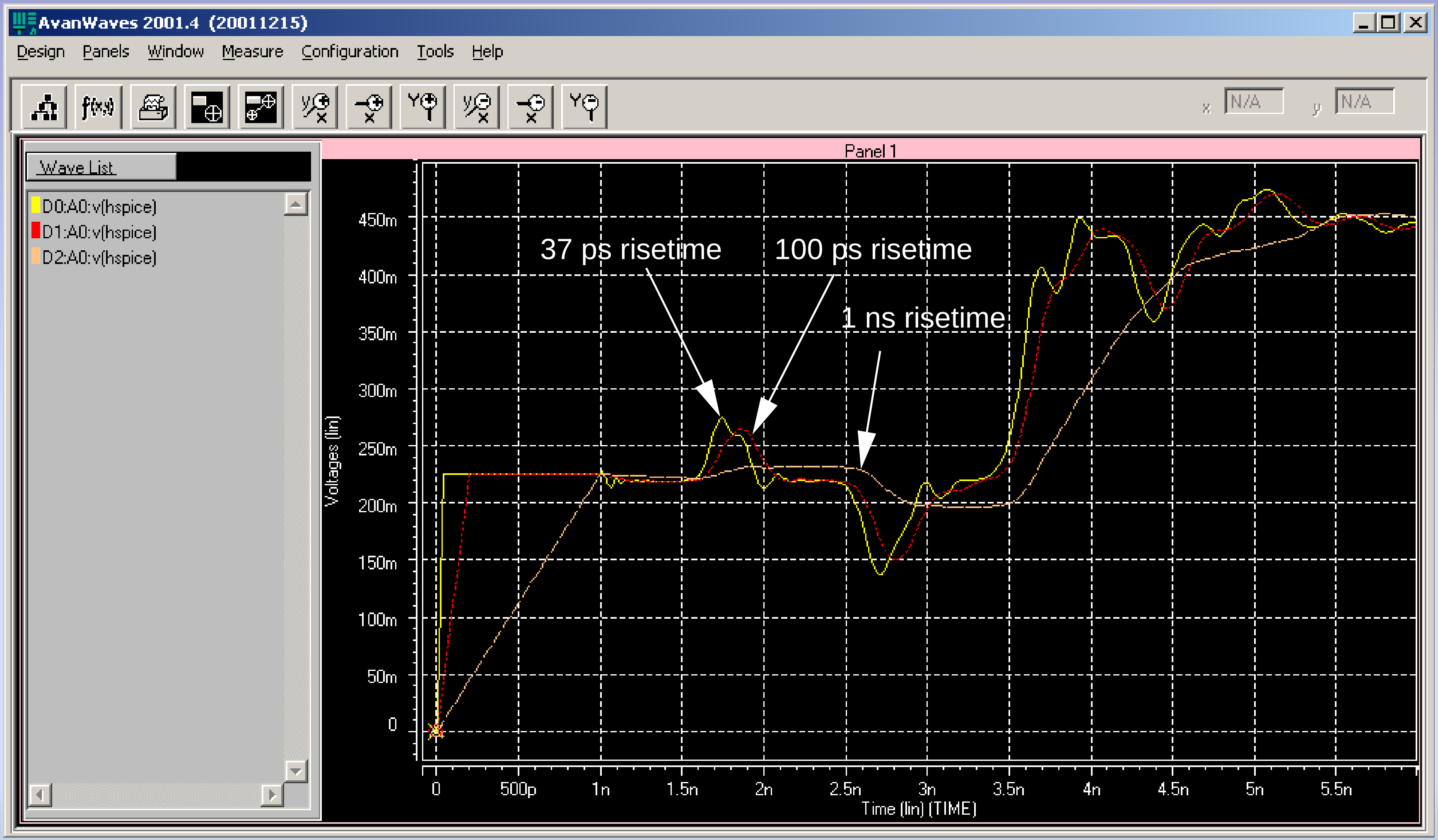


unfiltered: Zmin=30.95, Zmax=67.4



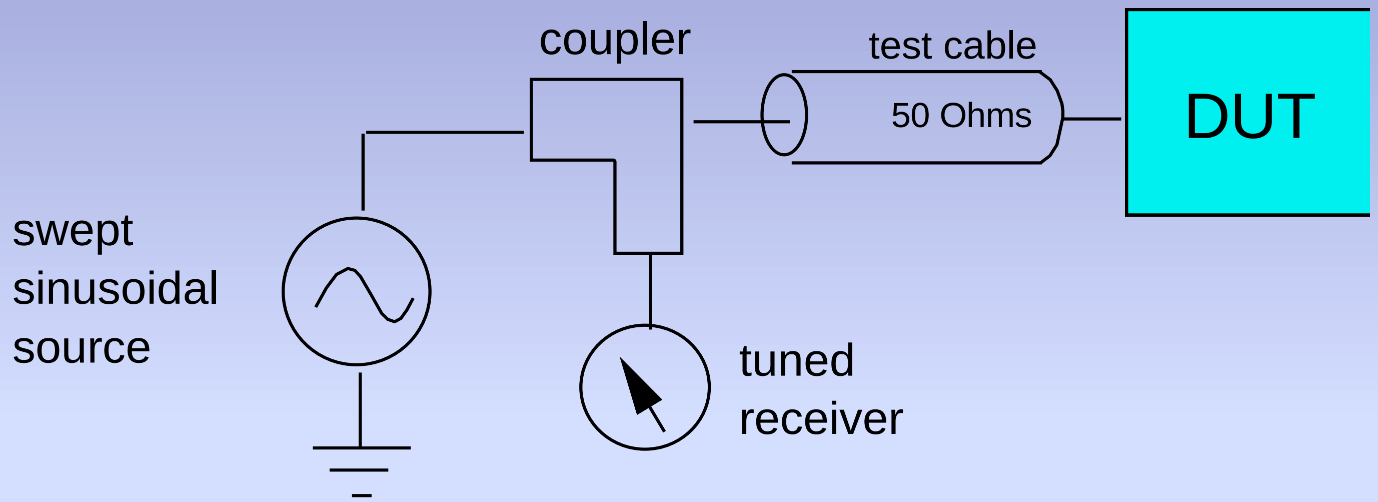
200 ps filter: Zmin=34.79, Zmax=61.98

"Ugly" network simulation



Impedance measurement

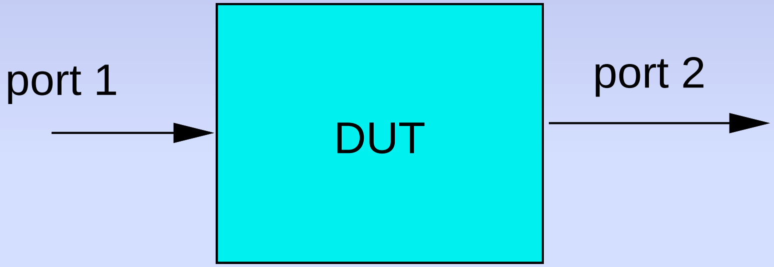
Vector Network Analyzer (VNA)



- freq. domain measurement - measures vs. frequency, typically. s parms.
- no spatial (distance) information
- can be single-ended (shown) or differential (if equipment capable)
- accuracy, resolution degrade with
  - loss in test cables and DUT
  - fixture effects, including discontinuities

s parameters

- Describe power transfer relationship between two ports of a DUT
- Normalized to 50 Ohms
- Can be related to other quantities; e. g., $Z1 = Z0 (1+s11)/(1-s11)$

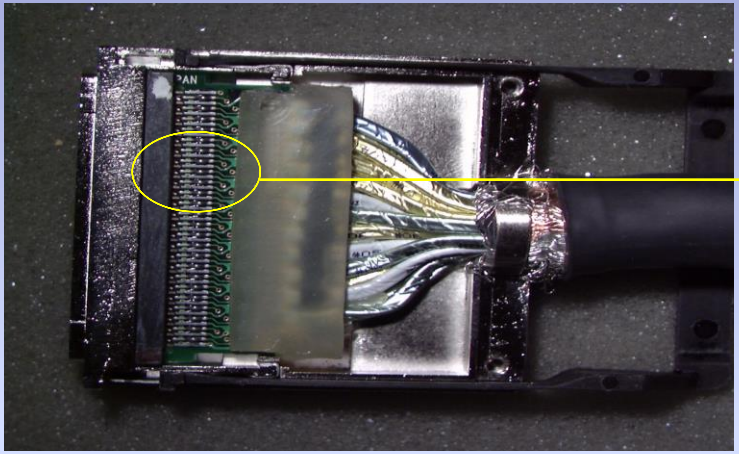


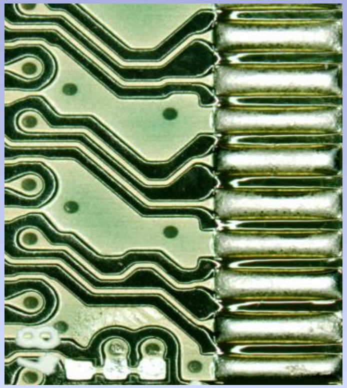
sxy = power observed at port x due to power applied at port y
s11 = return loss (reflection) at port 1
s21 = insertion loss, port 1 to port 2
s22 = return loss (reflection) at port 2

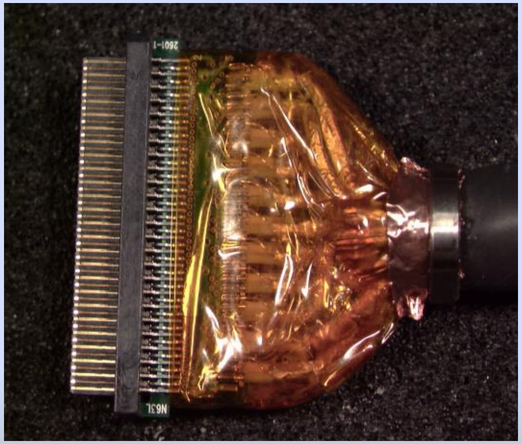
Impedance Discontinuities

- Change in geometry of conductors
  - width, thickness of signal conductor
  - proximity to reference plane
- Change in surrounding materials (ε_r)
  - plastic insulators, connector body in connectors
  - conductor dielectric, hot melt, overmold in cables

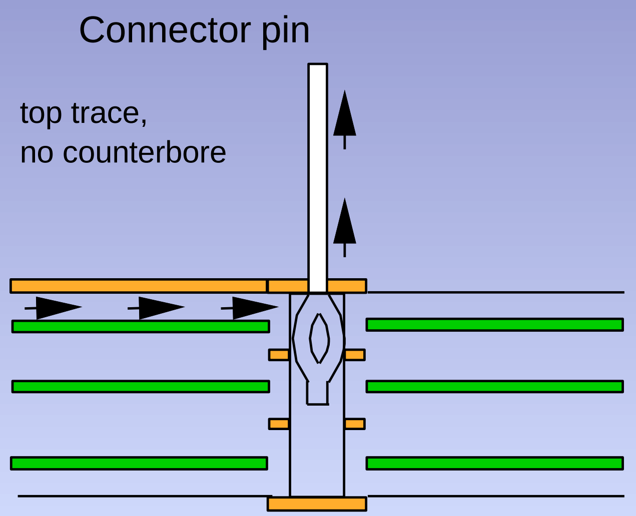
Impedance Discontinuities

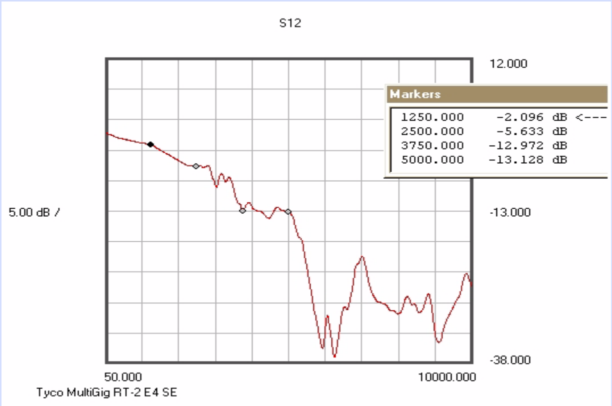






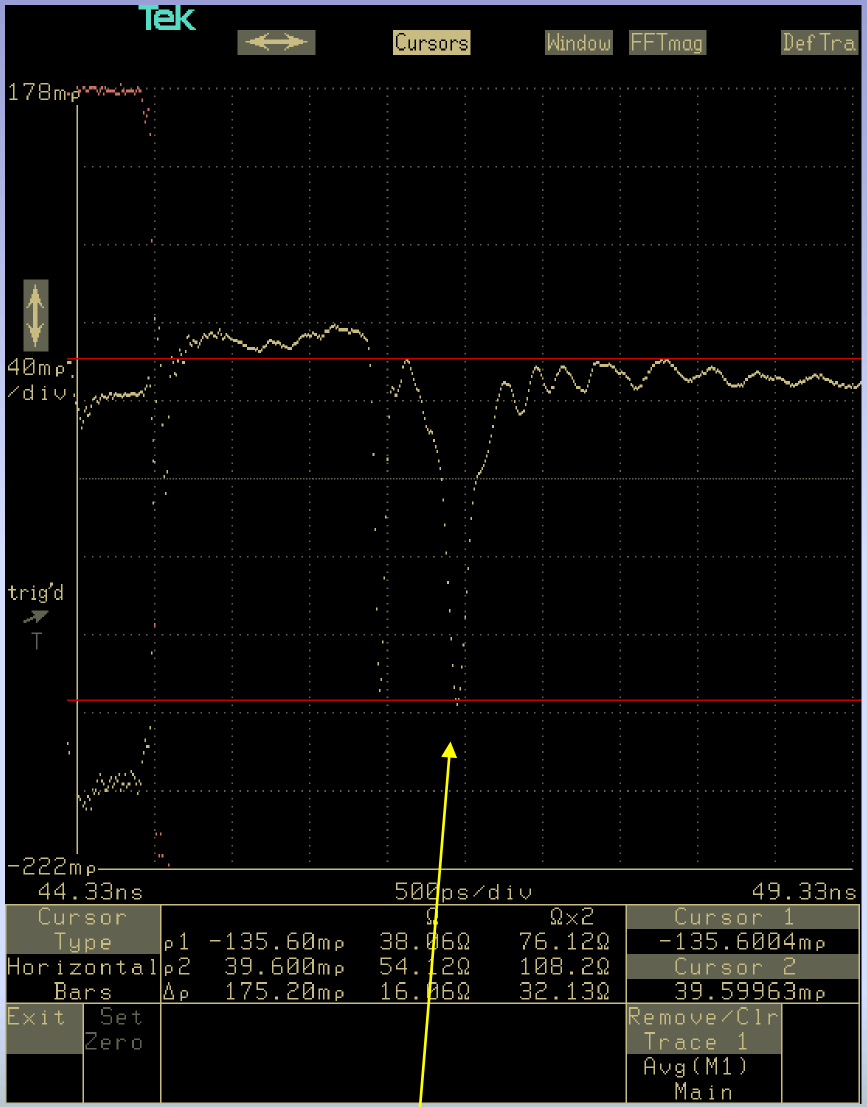
Vias





Insertion loss

1250.000	-2.096 dB <---
2500.000	-5.633 dB
3750.000	-12.972 dB
5000.000	-13.128 dB

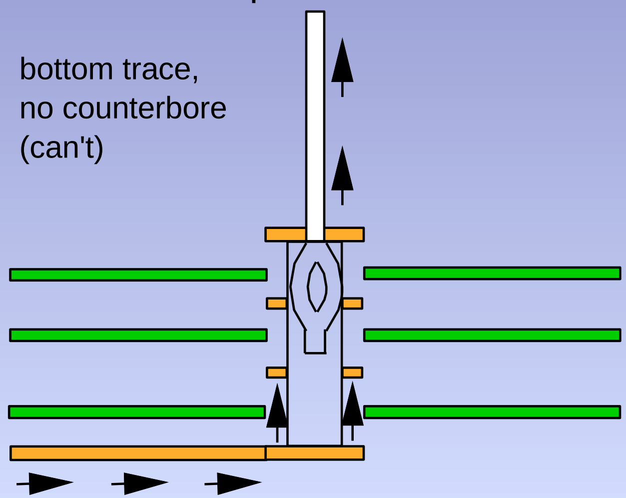


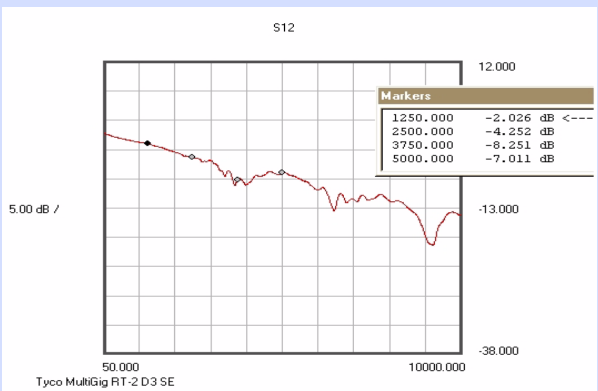
min. Z=38 Ohms

Vias

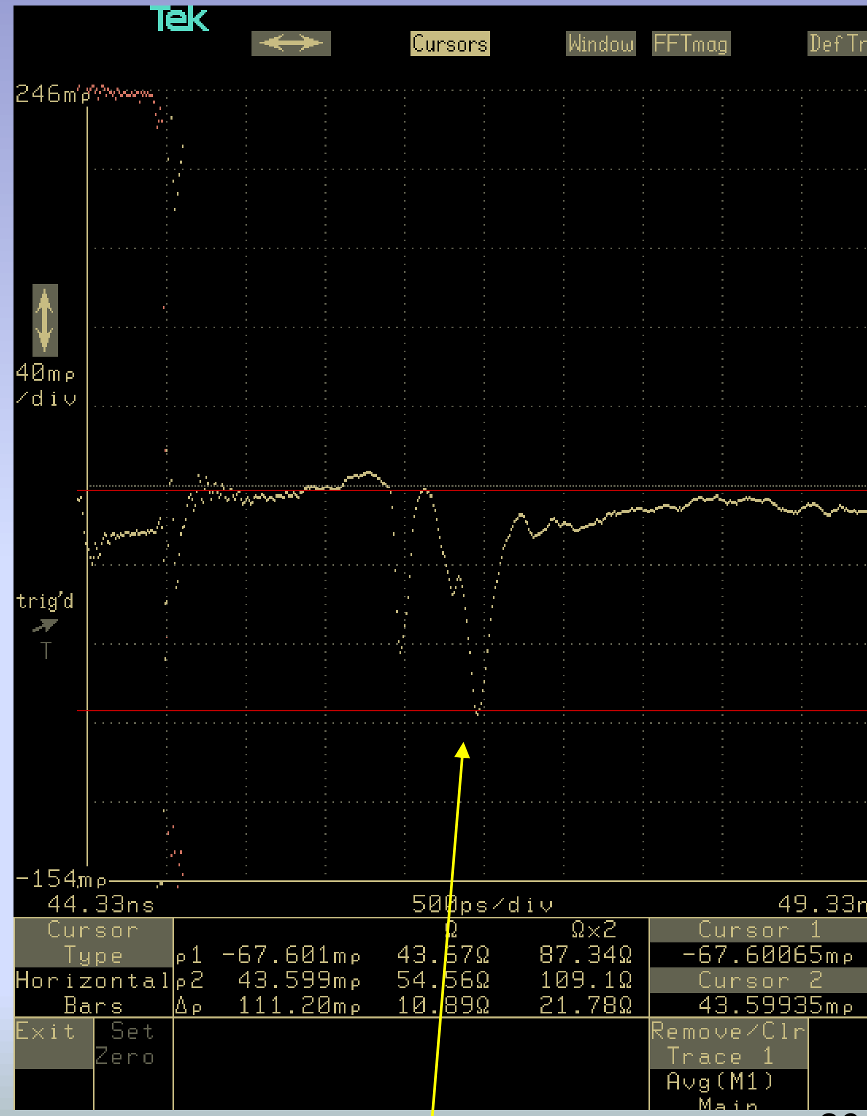
Connector pin

bottom trace,
no counterbore
(can't)





Insertion loss



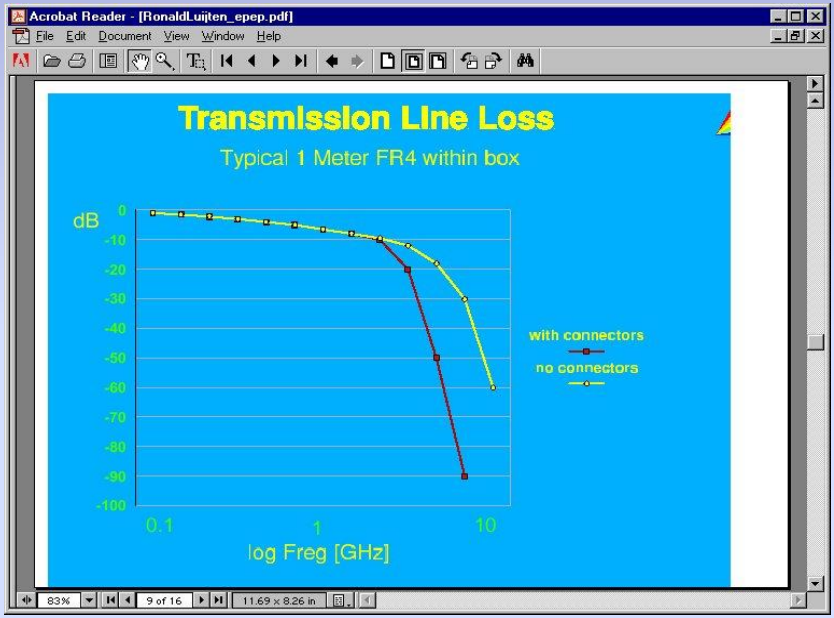
min. Z=44 Ohms

Impedance tools

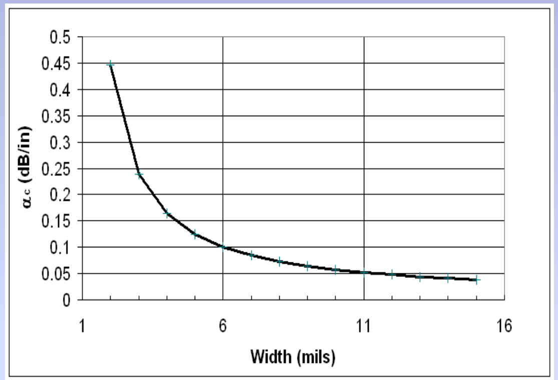
- Cadence Allegro SpectraQuest
- Mentor Graphics' Hyperlynx
- Missouri Univ. of Science & Tech. FEMAS
- IBM Yorktown EIP tools (CZ2D, EmitPkg)
- Polar Instruments (http://www.polarinstruments.com)
- HSPICE built-in field solver
- Ansys, Applied Simulation Technology, etc. field solvers
- Agilent AppCAD (http://www.agilent.com)
- Tektronix Iconnect^{tm}
- other free tools

Maximizing SI

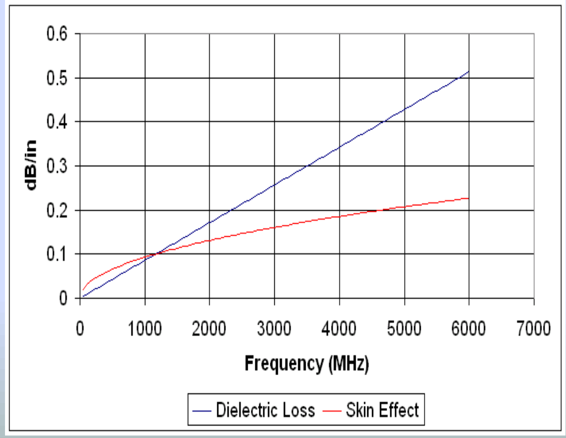
- Understand the channel
- Biggest culprit is frequency-dependent insertion loss (and reflections)
- Next problem is crosstalk



source: R. Luijten, IBM Zurich, 2000 EPEP Conf.



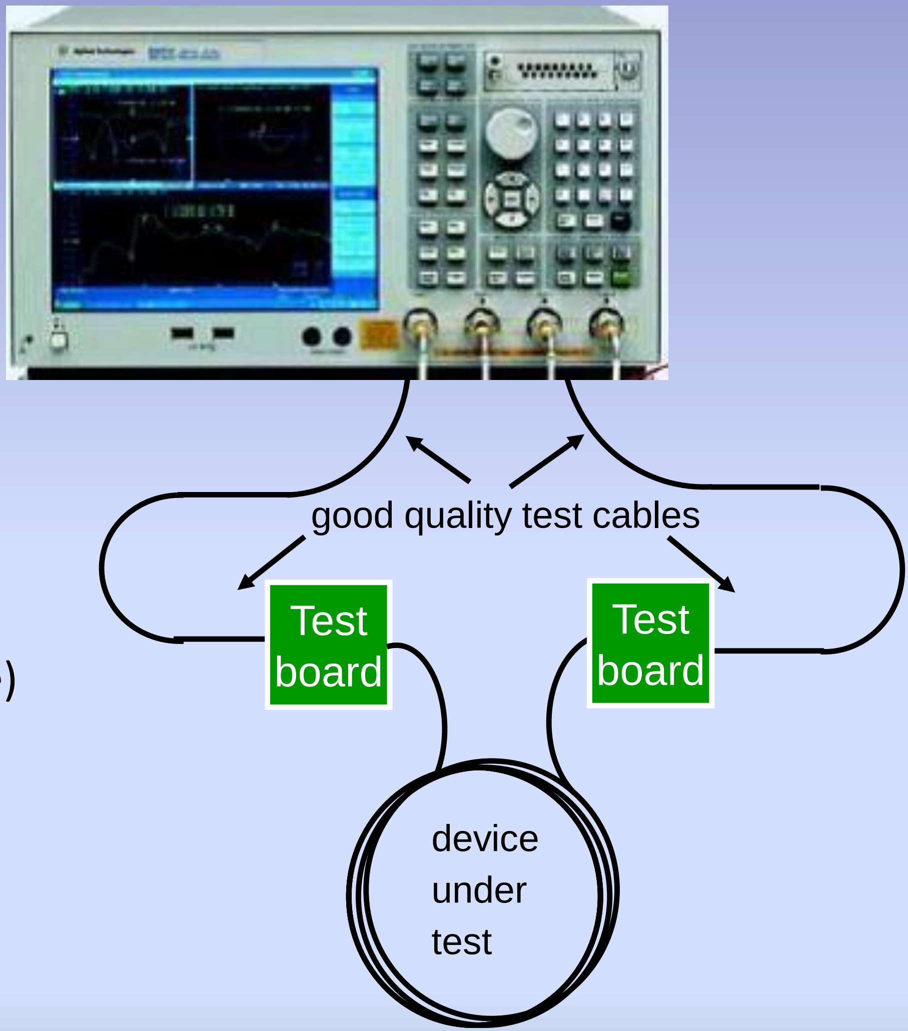
source: J. Cain, Cisco Systems, 2000 EPEP Conf.



- Minimize channel losses, reflections, crosstalk
- Equalize if necessary

Vector Network Analyzer

- Frequency-swept stimulus and response
- Two or more ports
- No location information
- Displays results in various formats
  - Log magnitude/phase
  - Smith Chart
  - Time domain (w/ software)



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- Ramo, S., Whinnery, J., and Van Duzer, T.: Fields and Waves in Communication Electronics, Wiley
- Young, Brian: Digital Signal Integrity Modeling and Simulation with Interconnects and Packages, Prentice-Hall
- http://www.murata.com - capacitor calculator
- http://www.te.com, www.molex.com - connector specs., papers on card wiring losses, via characteristics, etc.

Conferences

- DesignCon – February, in Santa Clara, CA
- IEEE Electrical Performance of Electronic Packaging (EPEP)
- IEEE EMC Symposium (EMCS)
    - in Raleigh, NC in August, 2014
    - Embedded SI conference
    - http://www.emcs.org
- IEEE ECTC, ED, ISSCC
- IEEE SPI workshop (Europe)

Conclusion

Please fill out the online evaluation form at http://www.emcs-dl.org/DL_Survey.php, using password EMCSDL

Thank you!