

The “Ground” Myth

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Outline

- Electromagnetics
- Skin Effect
- Inductance
- Ground
- Return Current Path

Electromagnetics

In the Beginning

- Electric and Magnetic effects not connected
- Electric and magnetic effects were due to ‘action from a distance’
- Faraday was the 1st to propose a relationship between electric lines of force and time-changing magnetic fields
 - Faraday was very good at experiments and ‘figuring out’ how things work

Maxwell



- Maxwell was impressed with Faraday's ideas
- Discovered the mathematical link between the “electro” and the “magnetic”
- Scotland's greatest contribution to the world (next to Scotch)

Maxwell's Equations – Differential Form

A difference in Magnetic Field
across a small piece of space

$$\nabla \times H = J + \frac{\partial D}{\partial t}$$

A change in
Electric Flux
Density with
respect to time

A difference in Electric Field
across a small piece of space

$$\nabla \times E = - \frac{\partial B}{\partial t}$$

A change in
Magnetic Flux
Density with
respect to time

Maxwell's Equations are not Hard!

- Change in H-field across space \approx Change in E-field (at that point) with time
- Change in E-field across space \approx Change in H-field (at that point) with time
- (Roughly speaking, and ignoring constants)

Current Flow

- Most important concept of EMC
- Current flow through metal changes as frequency increases
- DC current
 - Uses entire conductor
 - Only resistance inhibits current
- High Frequency
 - Only small part of conductor (near surface) is used
 - *Resistance* is small part of current inhibitor
 - **Inductance** is major part of current inhibitor

Skin Depth

- High frequency current flows only near the metal surface at high frequencies

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$$

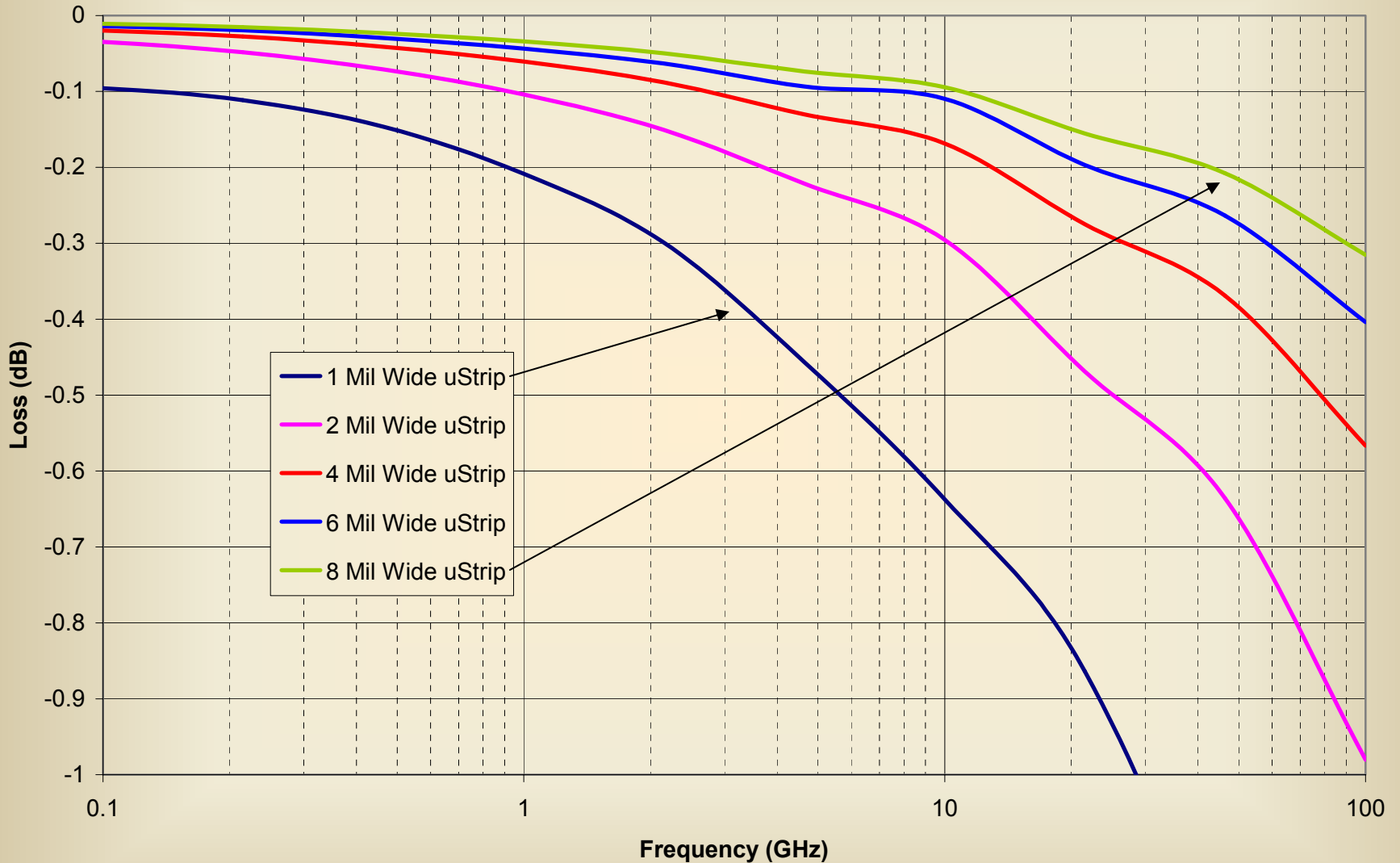
Frequency	Skin Depth	Skin Depth
60 Hz	260 mils	8.5 mm
1 KHz	82 mils	2.09 mm
10 KHz	26 mils	0.66 mm
100 KHz	8.2 mils	0.21 mm
1 MHz	2.6 mils	0.066 mm
10 MHz	0.82 mils	0.021 mm
100 MHz	0.26 mils	0.0066 mm
1 GHz	0.0823 mils	0.0021 mm

Current Migrates to Outer Portions of the Conductor at High Frequencies

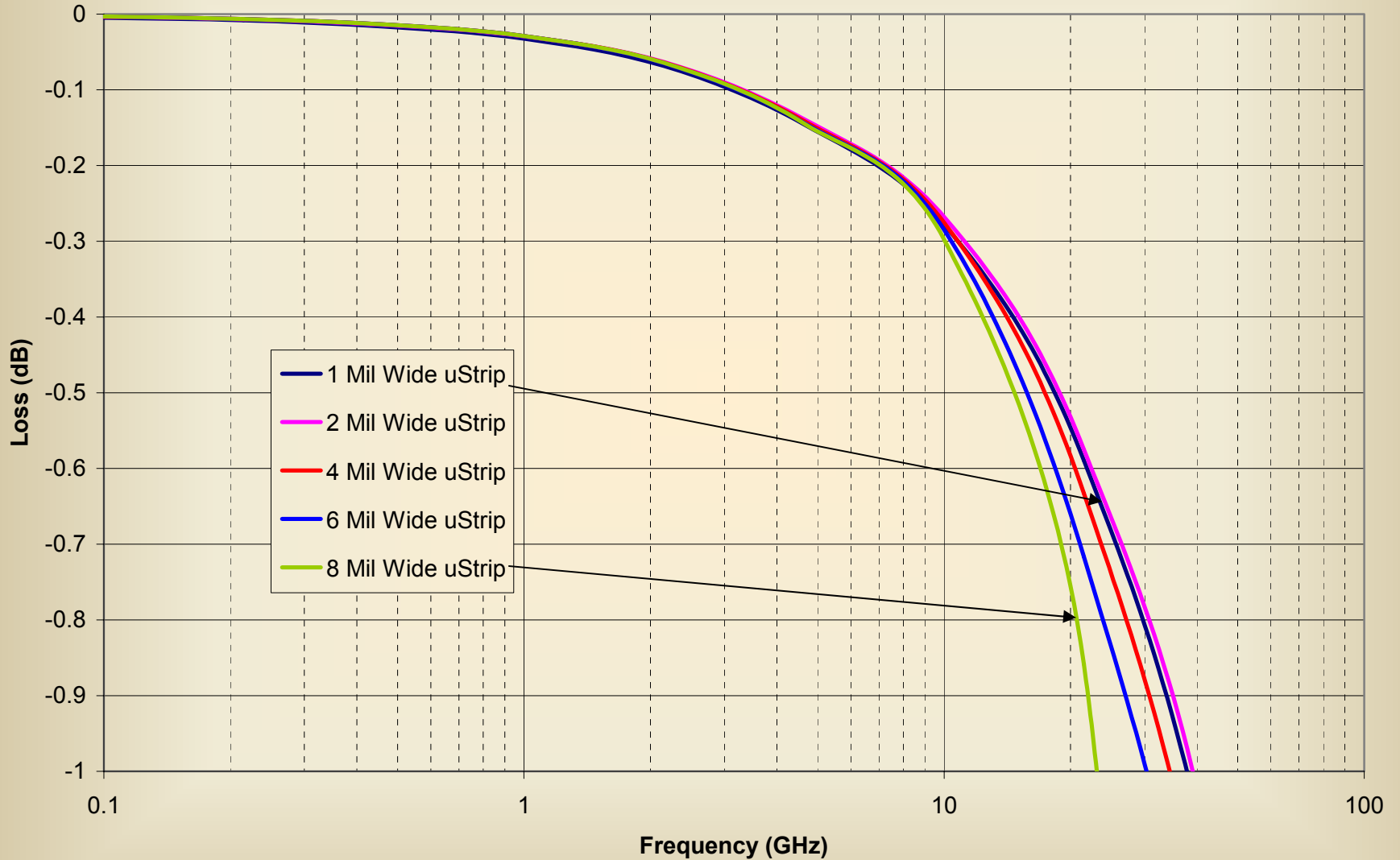


Resistance is determined by the area of the copper conductor actually used at each frequency!

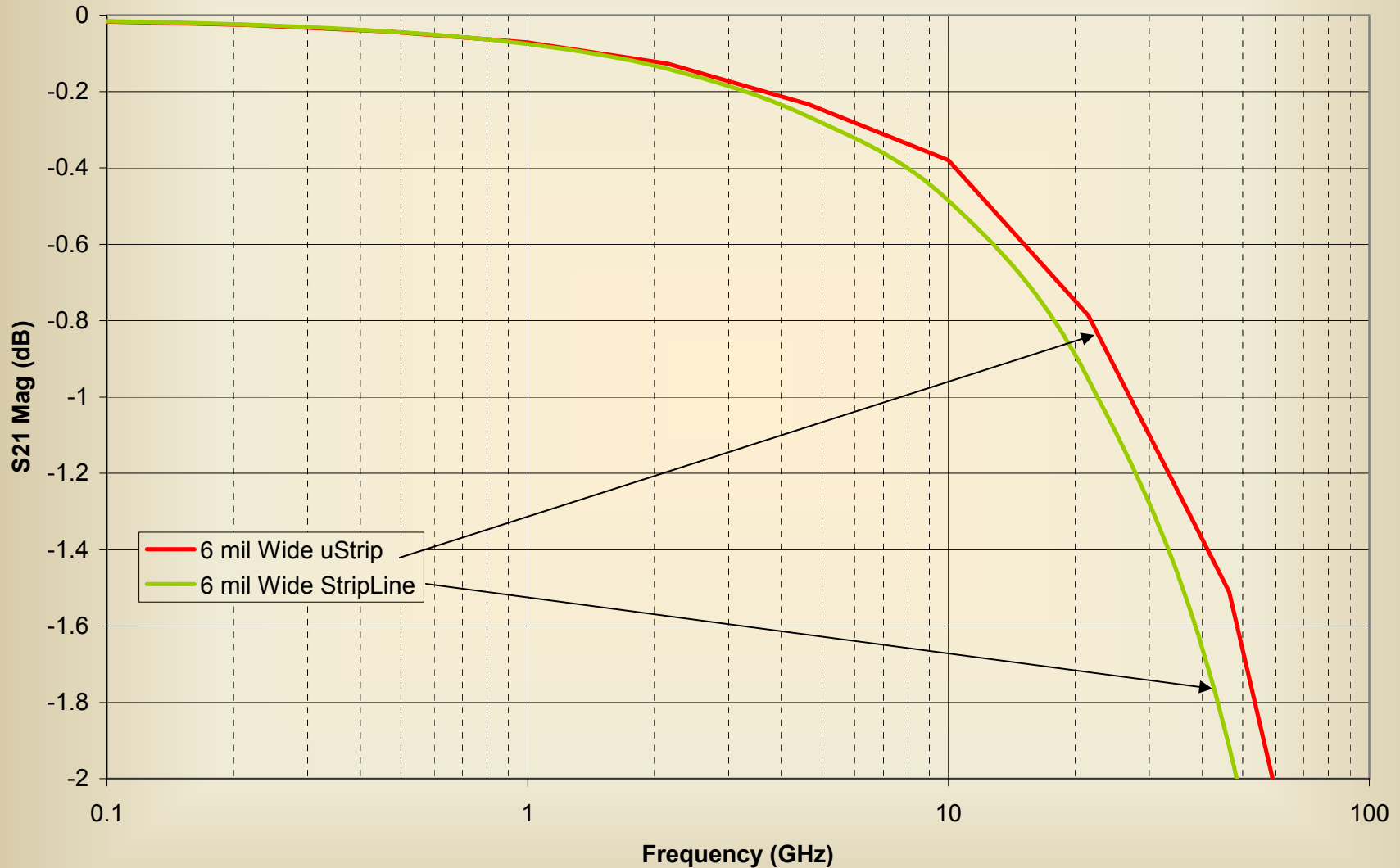
**S21 Skin Effect Loss ONLY-- Comparison for Microstrip (1 cm Long)
Various Widths -- 50 ohms (FR4, 4.2, 0.021) Trace Thickness = 0.6mil**



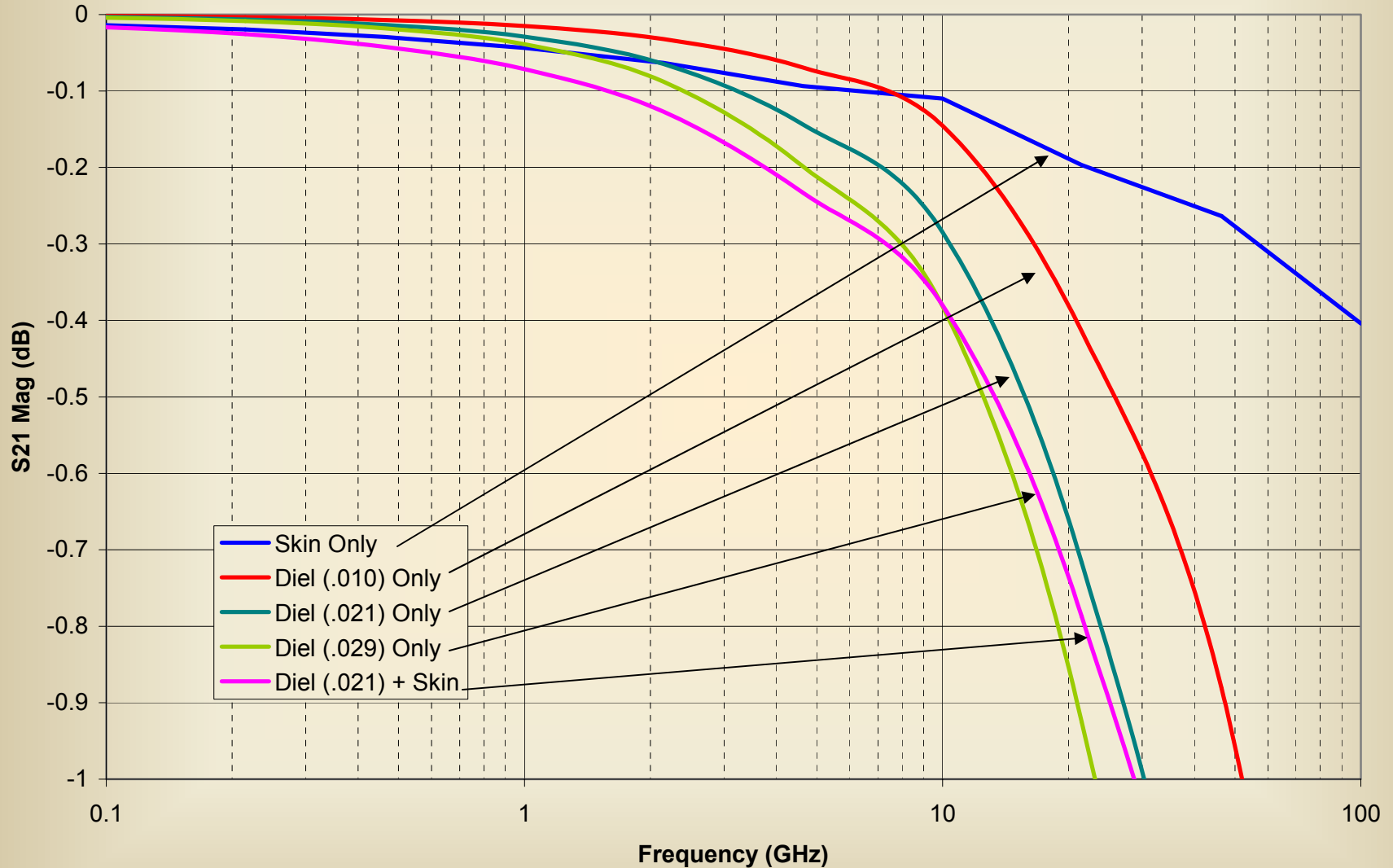
**S21 Dielectric Loss ONLY-- Comparison for Microstrip (1 cm Long)
Various Widths -- 50 ohms (FR4, 4.2, 0.021) Trace Thickness = 0.6mil**



S21 Loss Comparison Between Stripline and Microstrip (1 cm Long) 6 mil wide -- 50 ohms (FR4, 4.2, 0.021) Trace Thickness = 0.6mil



S21 Loss Comparison for 6 Mil Wide Microstrip Loss (1 cm Long) Various Dielectric Loss -- 50 ohms (FR4, 4.2) Trace Thickness = 0.6mil



At High Frequencies

- Resistive loss and dielectric loss are present
- Inductance will usually dominate

Inductance

- Current flow through metal => inductance!
- Fundamental element in EVERYTHING
- Loop area first order concern
- Inductive impedance increases with frequency and is MAJOR concern at high frequencies

$$X_L = 2\pi fL$$

Current Loop \Rightarrow Inductance



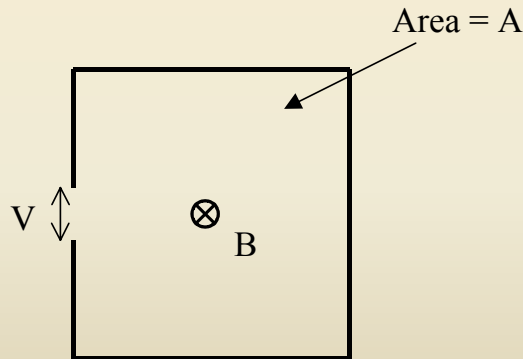
Courtesy of Elya Joffe

Inductance Definition

- Faraday's Law

$$\oint \vec{E} \cdot d\vec{l} = - \iint \frac{\partial \vec{B}}{\partial t} \cdot d\vec{S}$$

- For a simple rectangular loop



$$V = -A \frac{\partial B}{\partial t}$$

The minus sign means that the induced voltage will work against the current that originally created the magnetic field!

Self Inductance

- Isolated circular loop $L \approx \mu_0 a \left(\ln \frac{8a}{r_0} - 2 \right)$

- Isolated rectangular loop

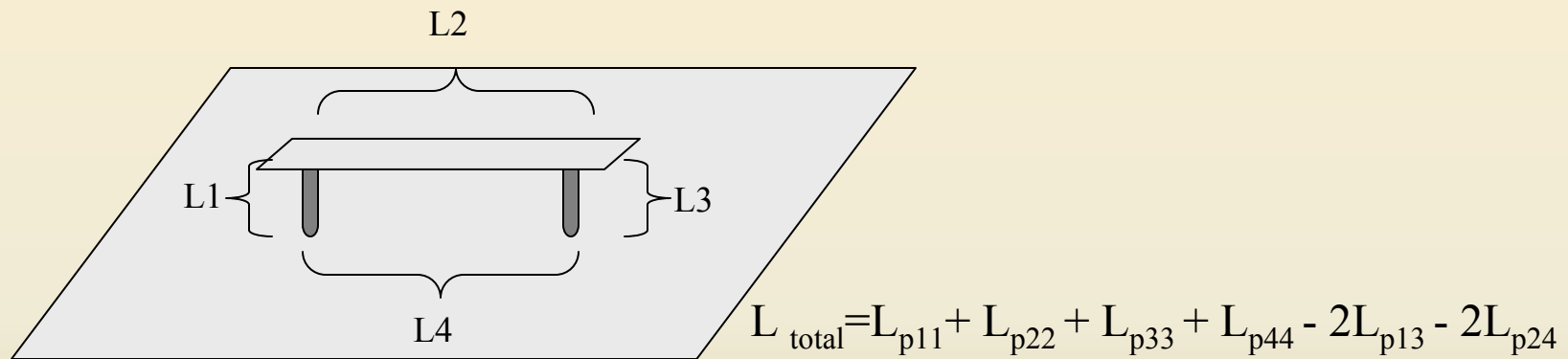
$$L = \frac{2\mu_0 a}{\pi} \left(\ln \frac{p + \sqrt{1 + p^2}}{1 + \sqrt{2}} + \frac{1}{p} - 1 + \sqrt{2} - \frac{1}{p} \sqrt{1 + p^2} \right)$$

Note that inductance is directly influenced by loop **AREA** and only less influenced by conductor size!

$$p = \frac{\text{length of side}}{\text{wire radius}}$$

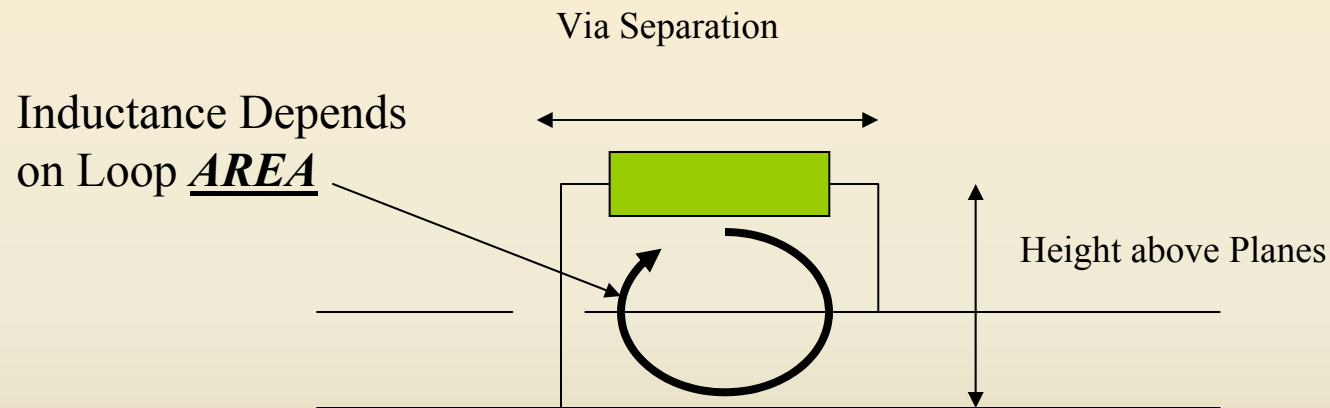
Partial Inductance

- Simply a way to break the overall loop into pieces in order to find total inductance



Decoupling Capacitor Mounting

- Keep as to planes as close to capacitor pads as possible



Important Points About Inductance

- Inductance is everywhere
- Loop area most important
- Inductance is everywhere

'Ground'

- **Ground is a place where potatoes and carrots thrive!**
- 'Earth' or 'reference' is more descriptive
- Original use of "GROUND"
- Inductance is everywhere

$$X_L = 2\pi fL$$



What we Really Mean when we say 'Ground'

- Signal Reference
- Power Reference
- Safety Earth
- Chassis Shield Reference

'Ground' is NOT a Current Sink!

- Current leaves a driver on a trace and must return (somehow) to its source
- This seems basic, but it is often forgotten, and is most often the cause of EMC problems



'Grounding' Needs Low Impedance at Highest Frequency

- Steel Reference Plate
 - 4 milliohms/sq @ 100KHz
 - 40 milliohms/sq @ 10 MHz
 - 400 milliohms/sq @ 1 GHz
- A typical via is about 2 nH
 - @ 100 MHz $Z = 1.3$ ohms
 - @ 500 MHz $Z = 6.5$ ohms
 - @ 1000 MHz $Z = 13$ ohms
 - @ 2000 MHz $Z = 26$ ohms

Single-point 'Ground'?

Vs

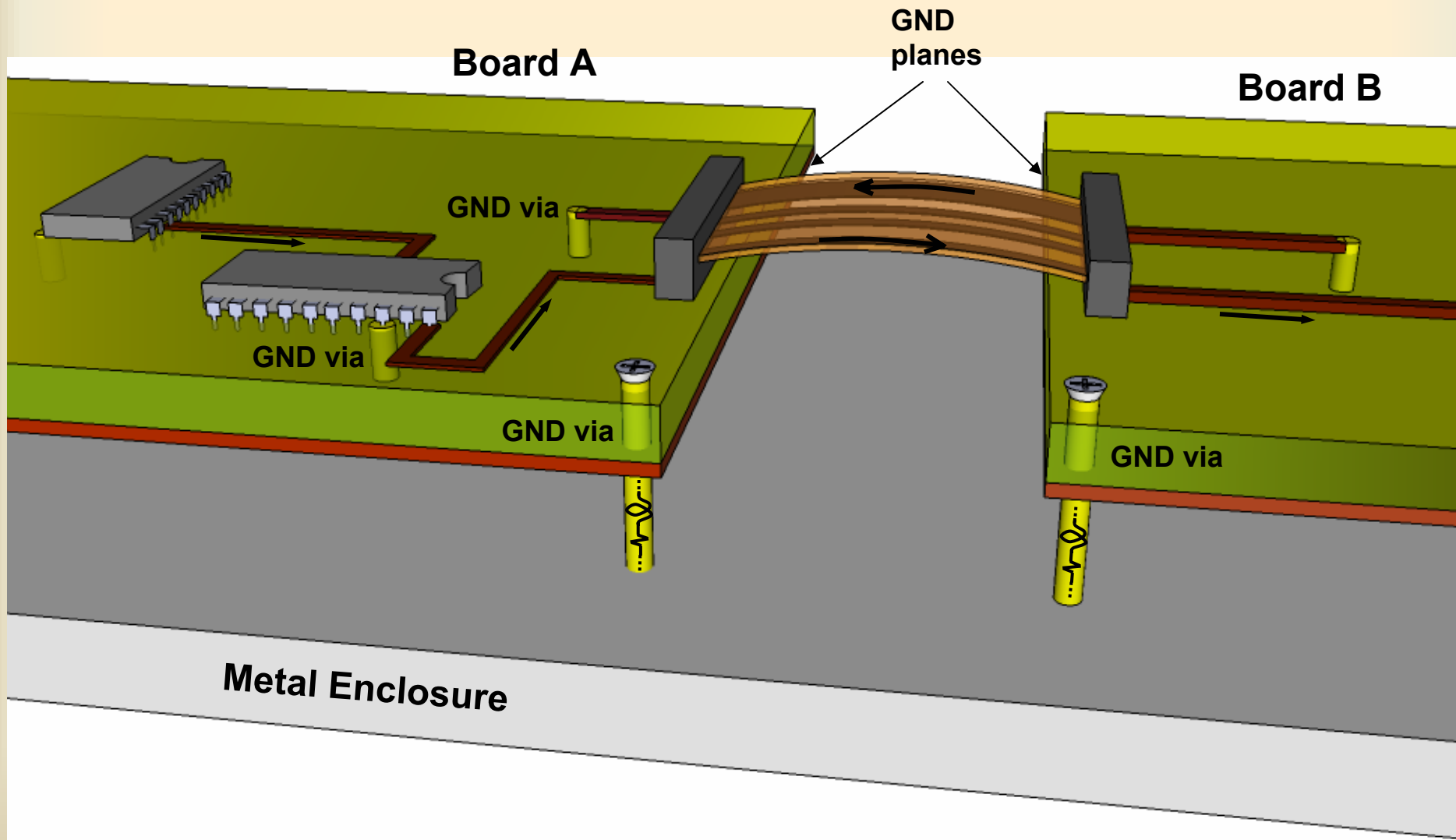
Multi-point 'Ground'?

- Which do I *want*?
- Which do I *get*?

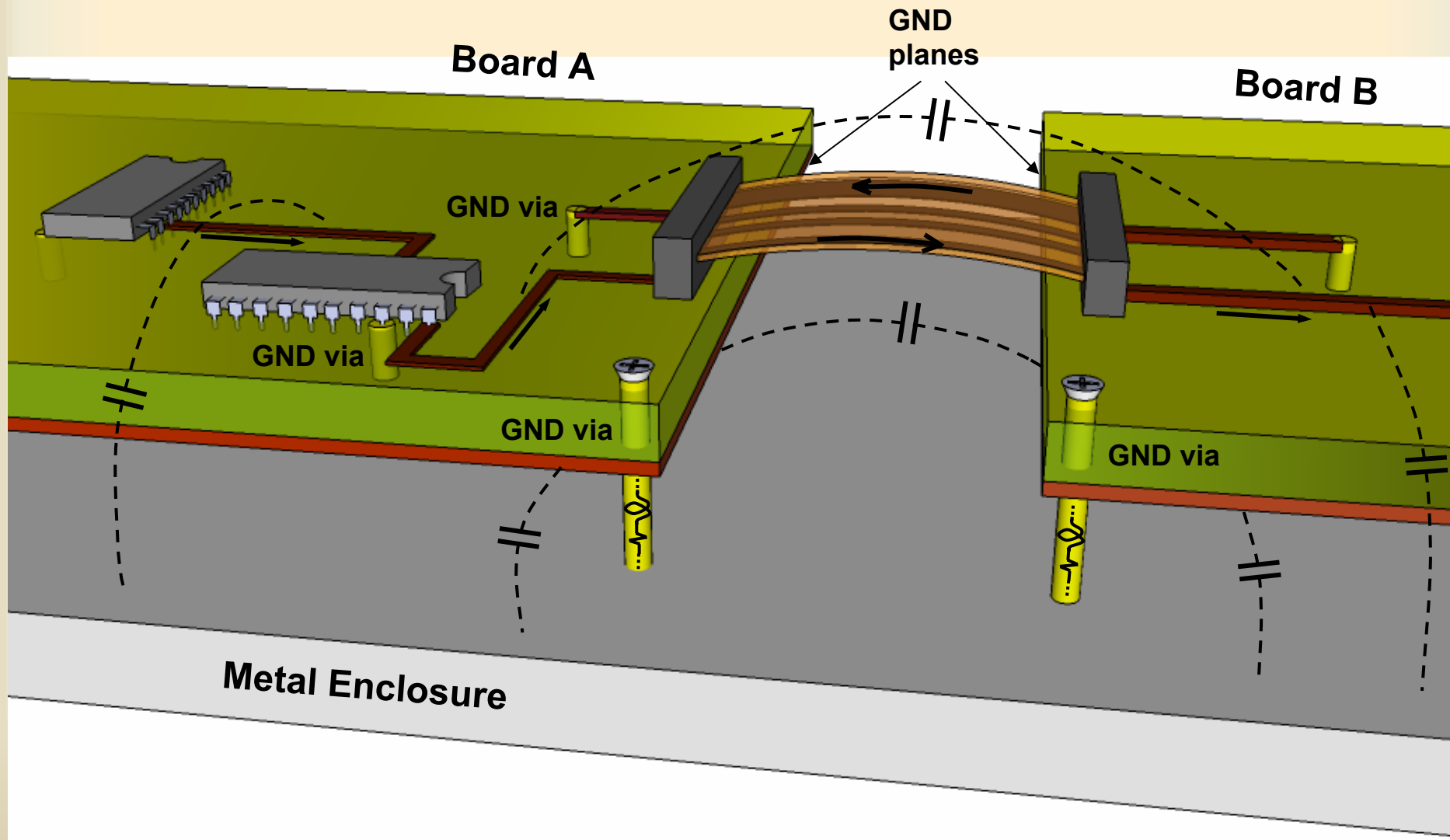
Single Point 'Ground' Myth

- At high frequencies, inductance makes this impossible!
- At high frequencies, parasitic capacitance makes this impossible!
- Depends on the amount of 'Ground' error your system can stand.....

Single-Point Ground Concept

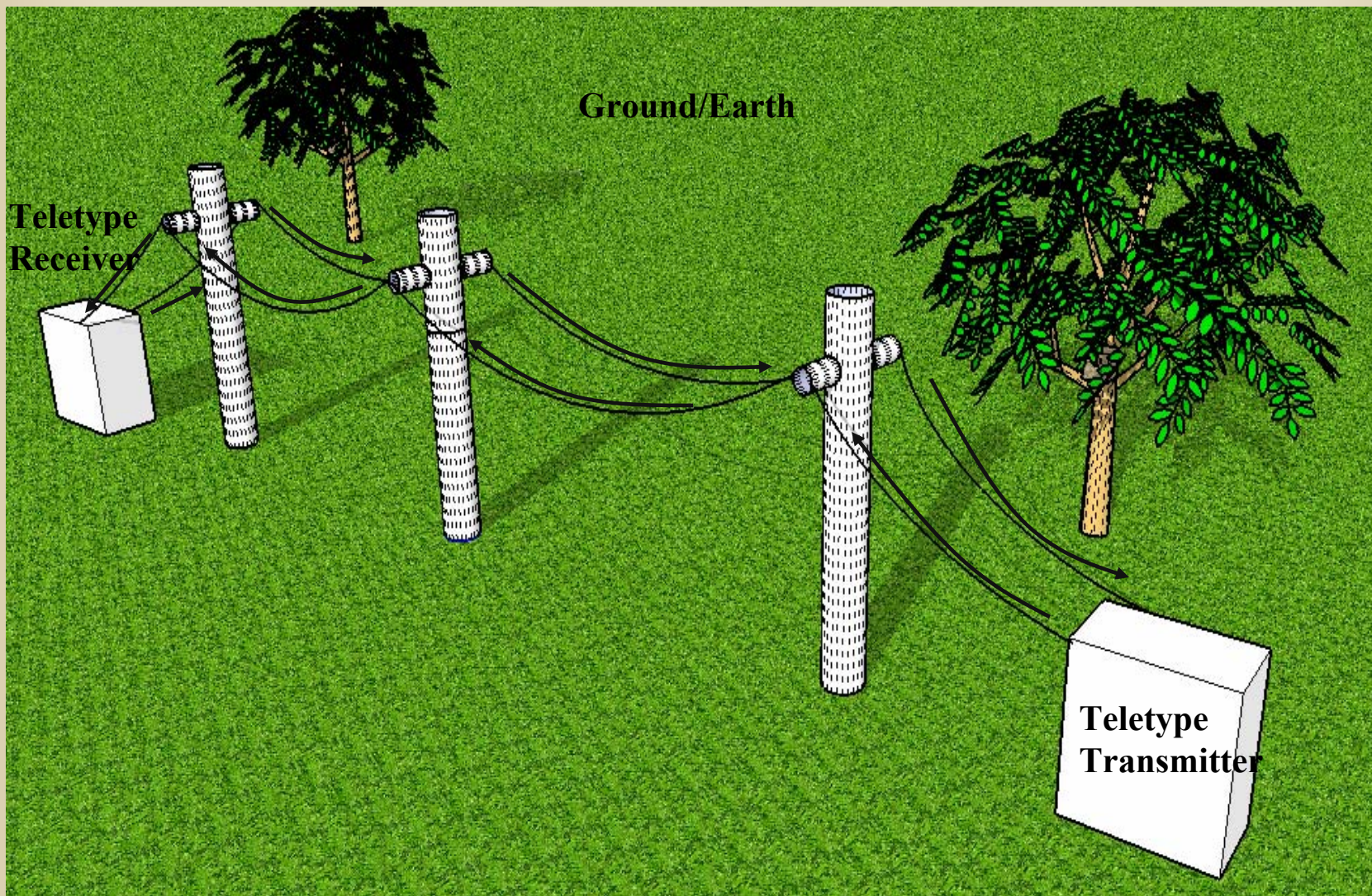


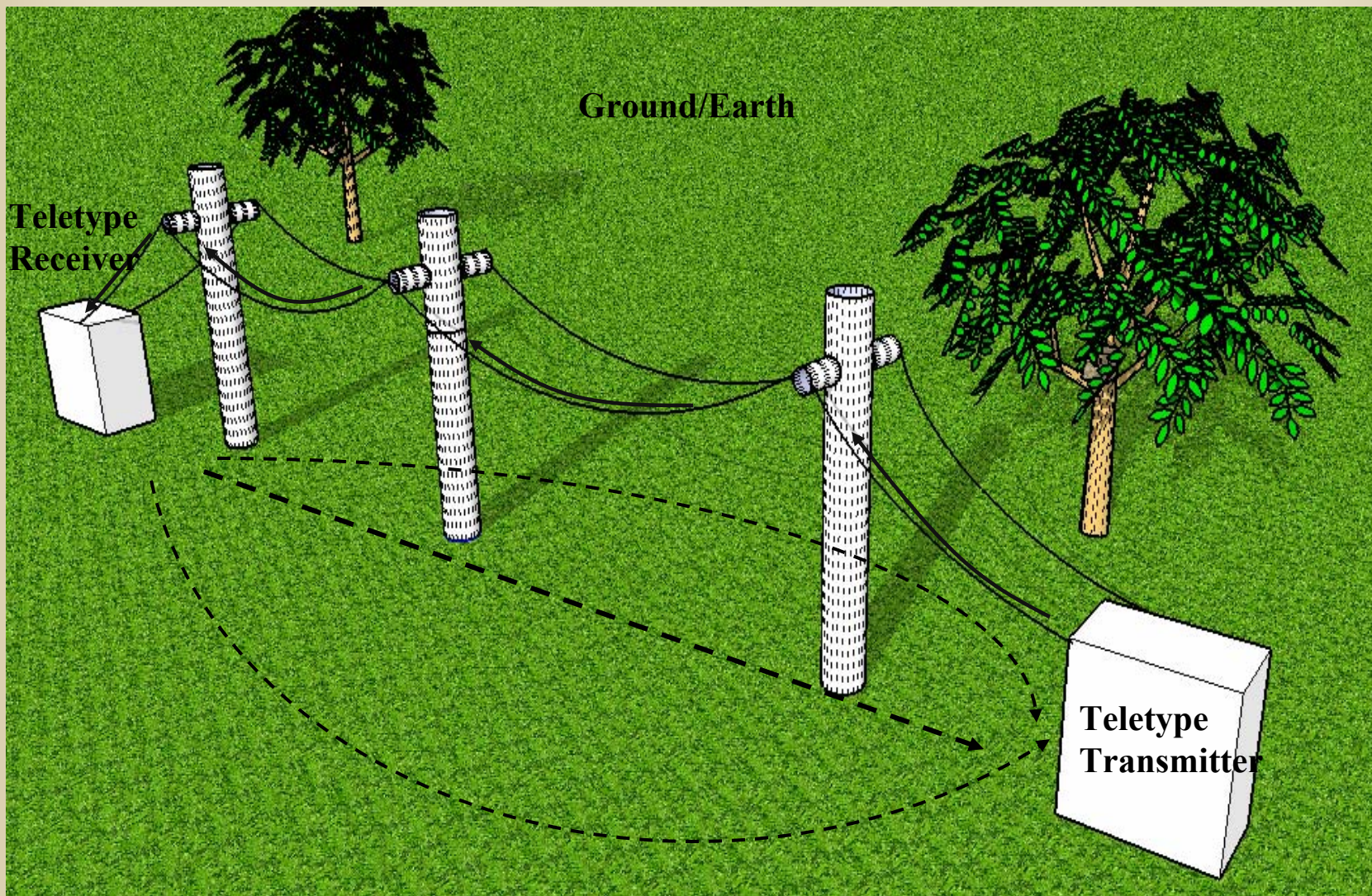
Reality Overcomes Single-Point Ground Intentions



Where did the Term “GROUND” Originate?

- Original Teletype connections
- Lightning Protection





Lightning striking house



Lightning

Lightning effect without rod



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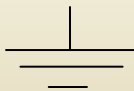
34

Lightning effect with rod

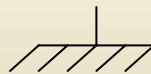


What we Really Mean when we say 'Ground'

- Signal Reference
- Power Reference
- Safety Earth
- Chassis Shield Reference



Circuit
"Ground"



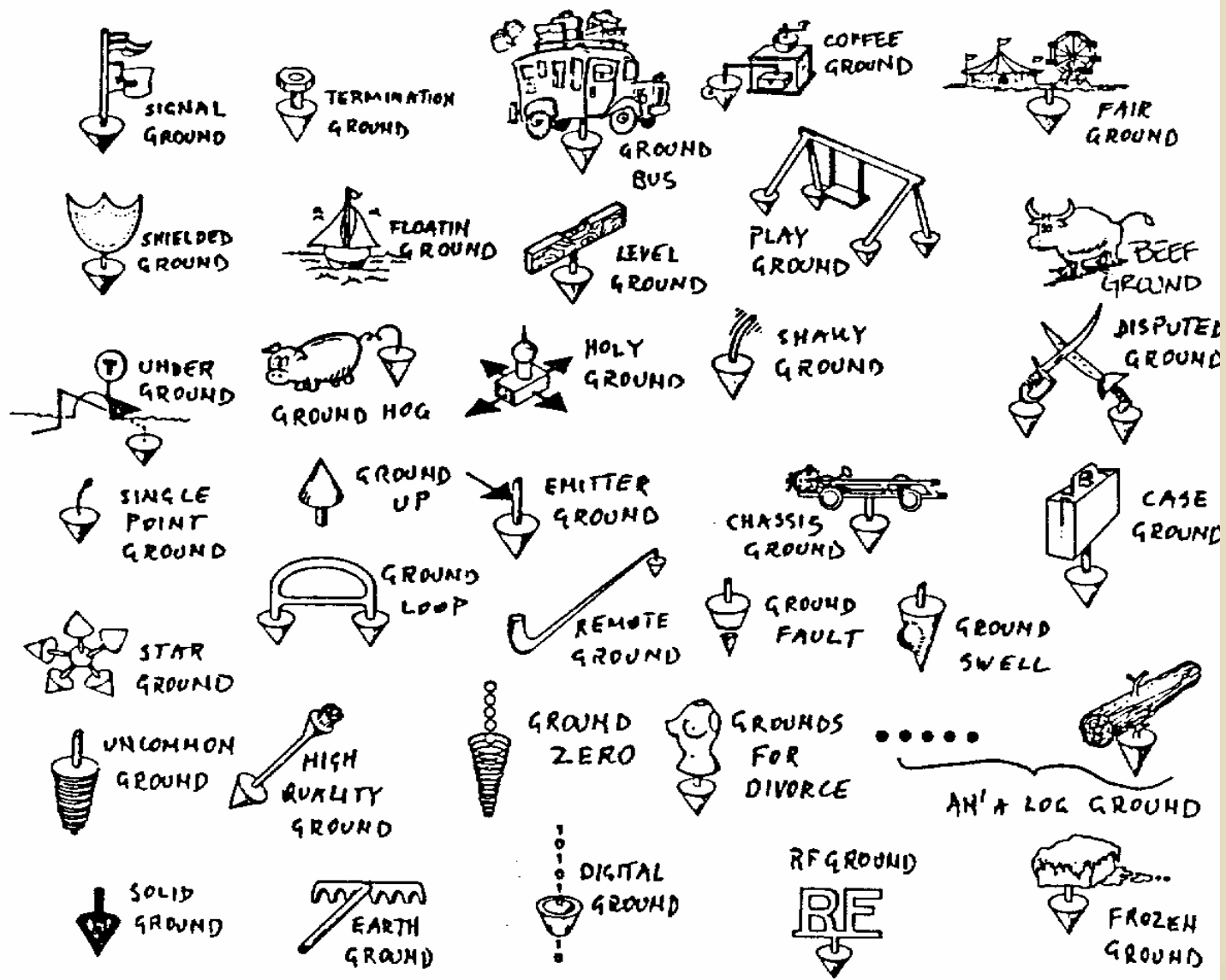
Chassis
"Ground"



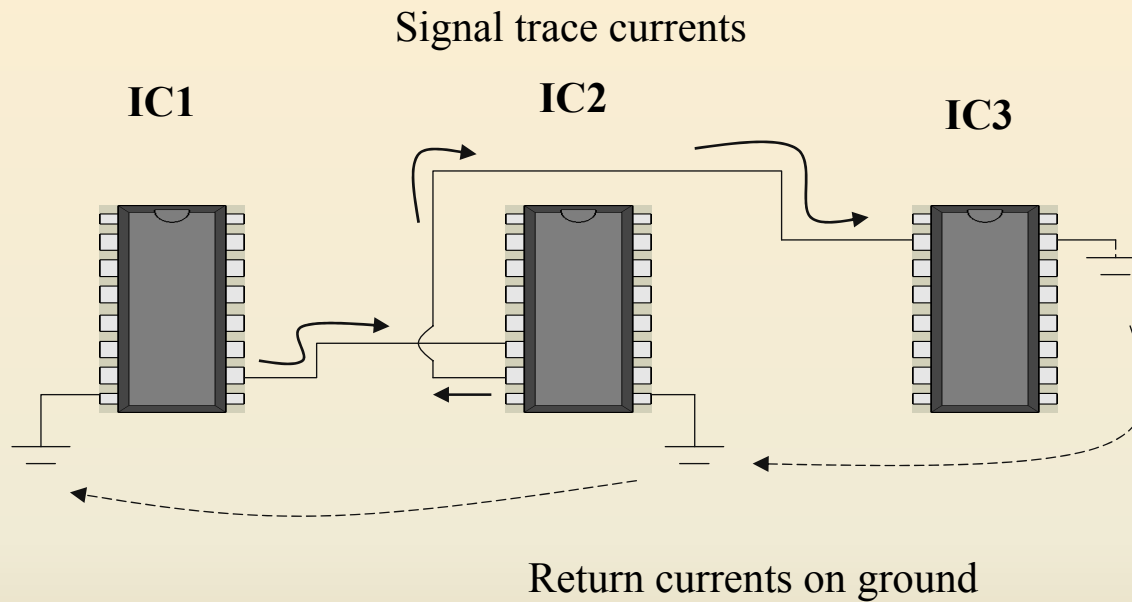
Digital
"Ground"



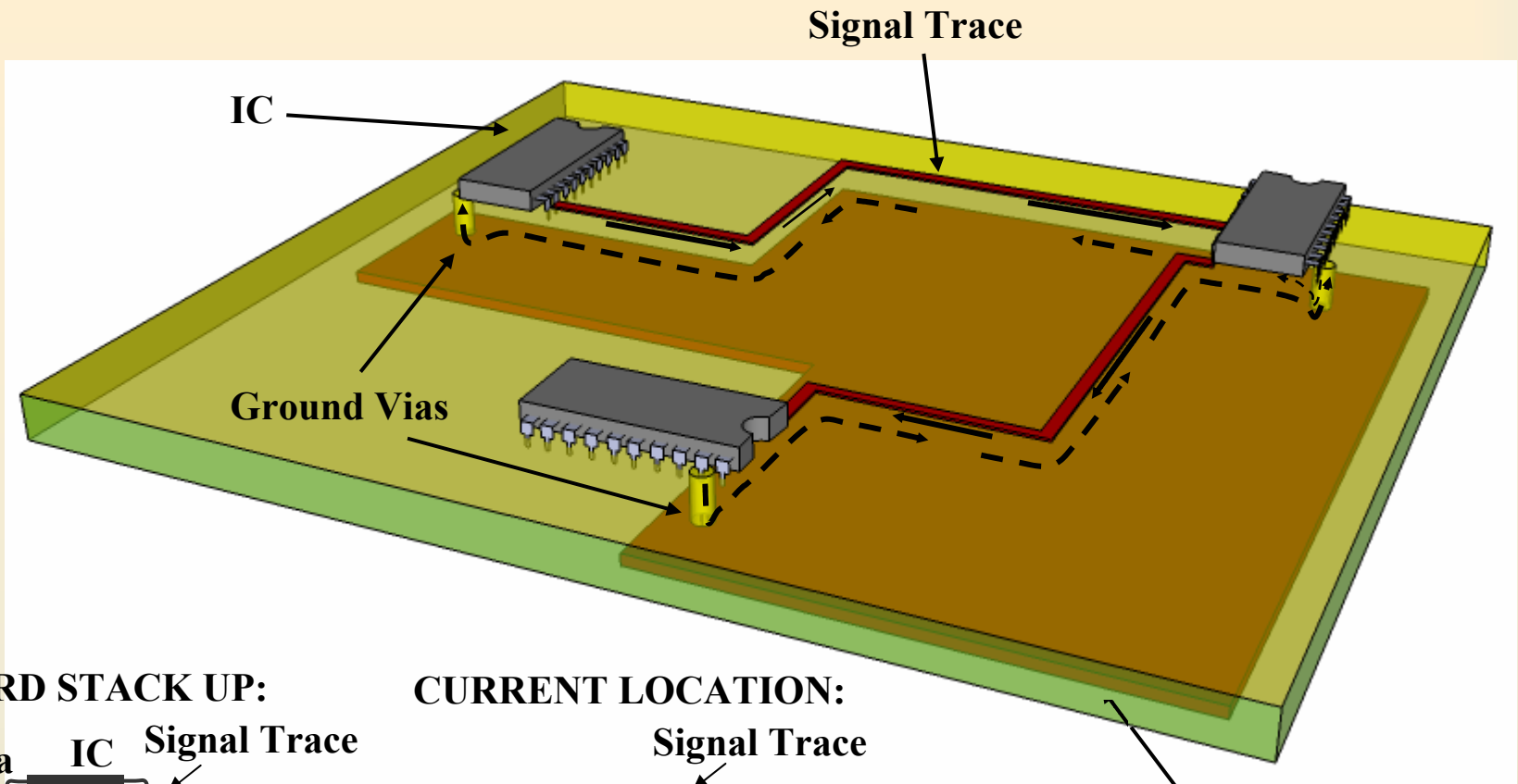
Analog
"Ground"



Schematic with Return Current Shown

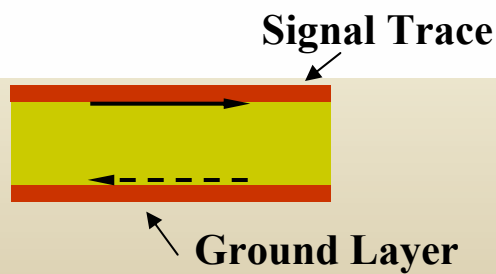
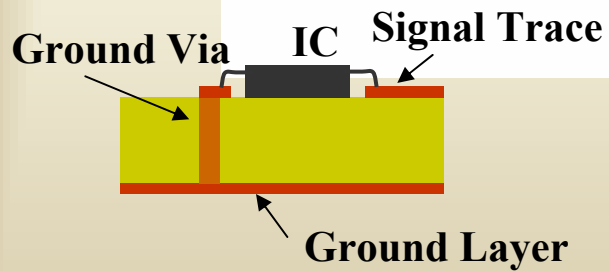


Actual Current Return is 3-Dimensional

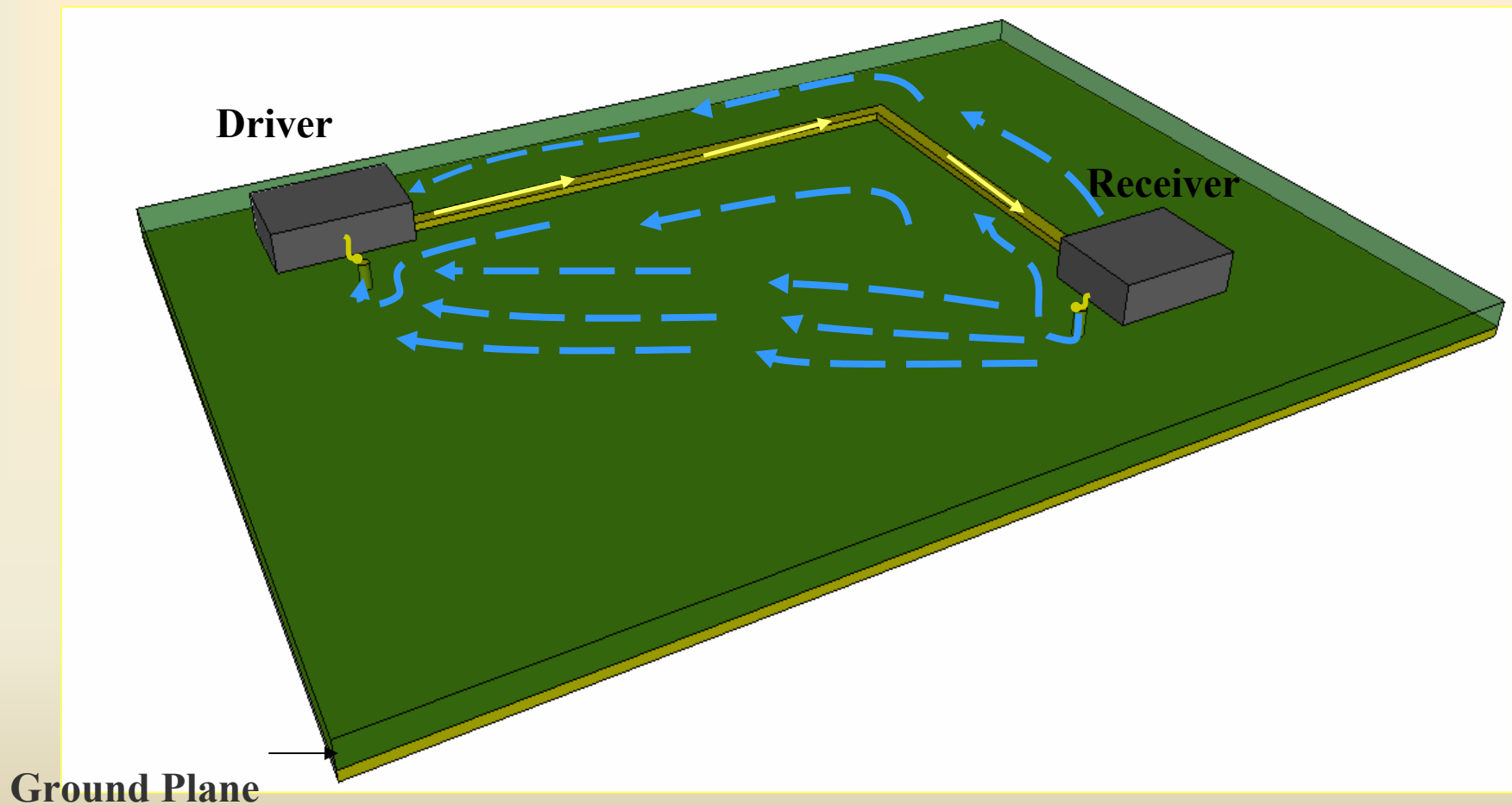


BOARD STACK UP:

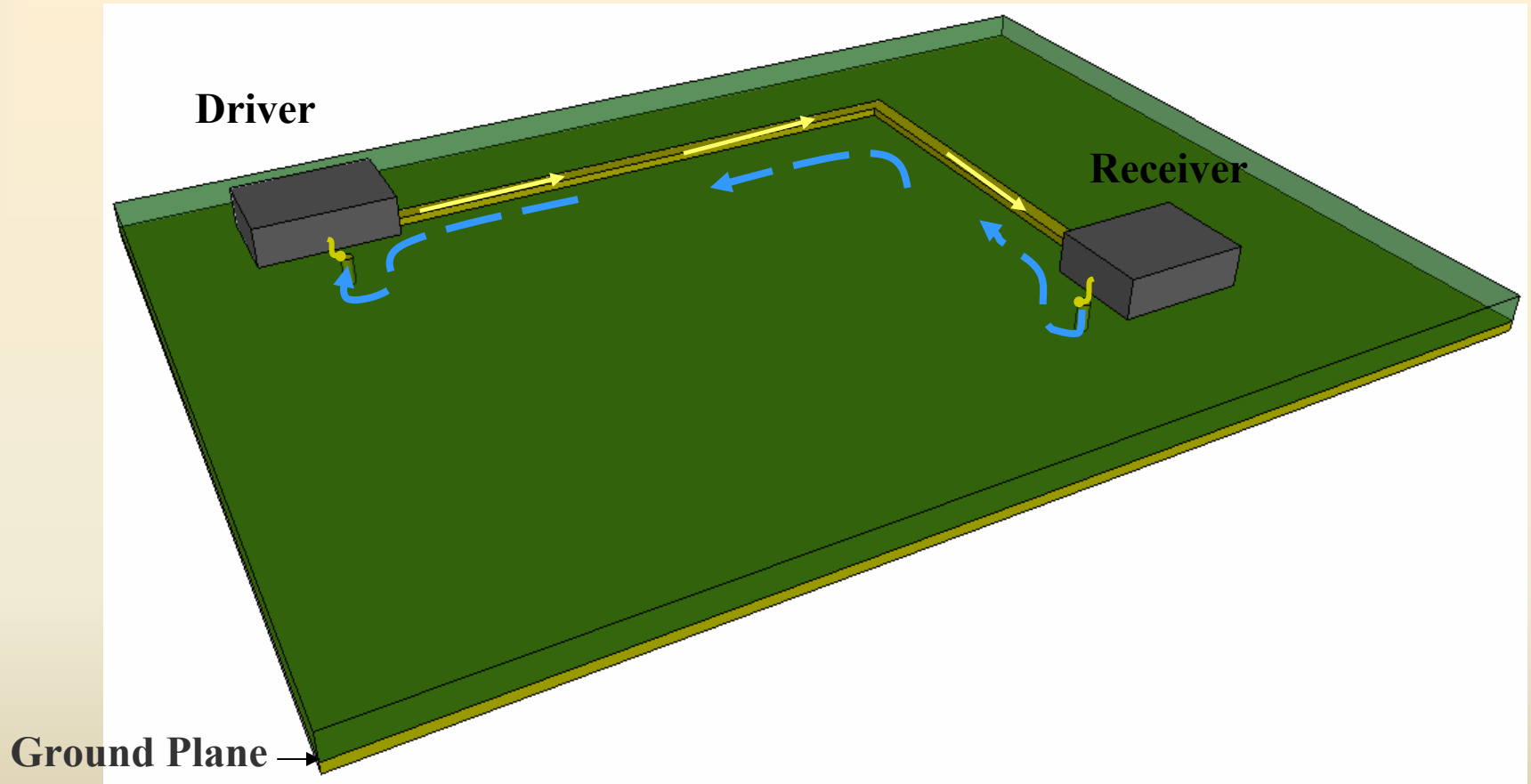
CURRENT LOCATION:



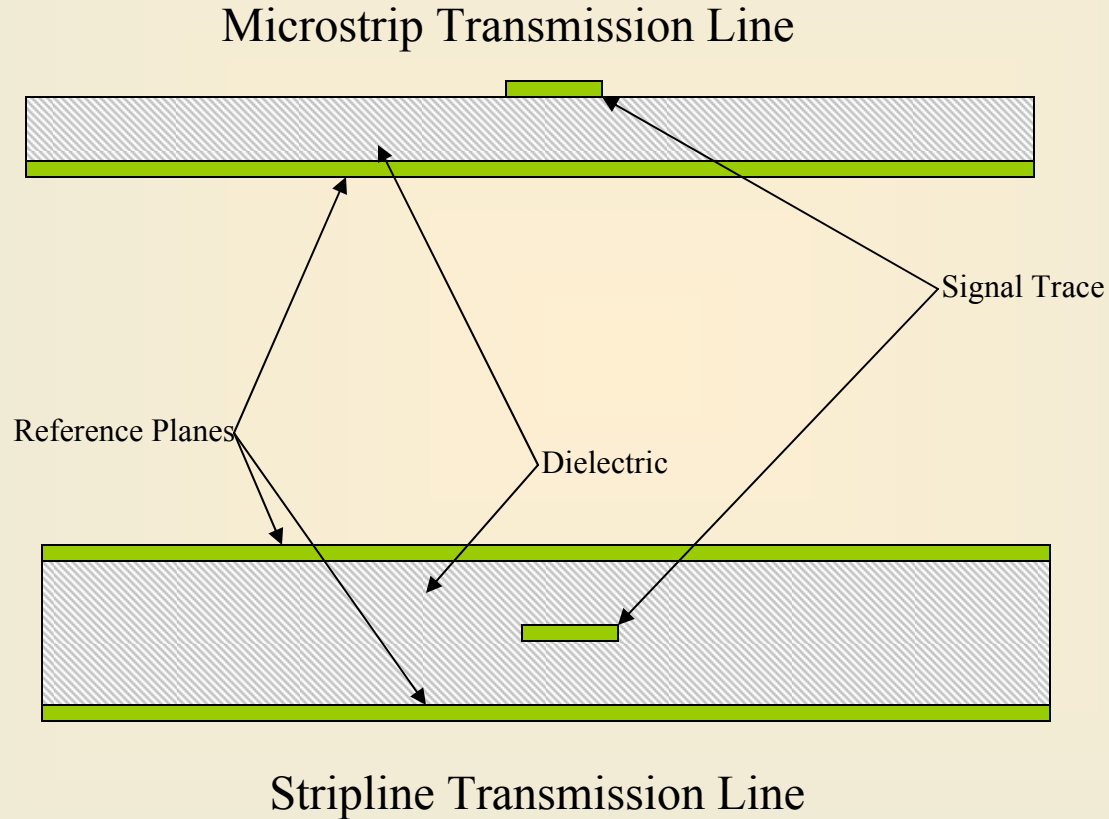
Low Frequency Return Currents Take Path of Least **Resistance**



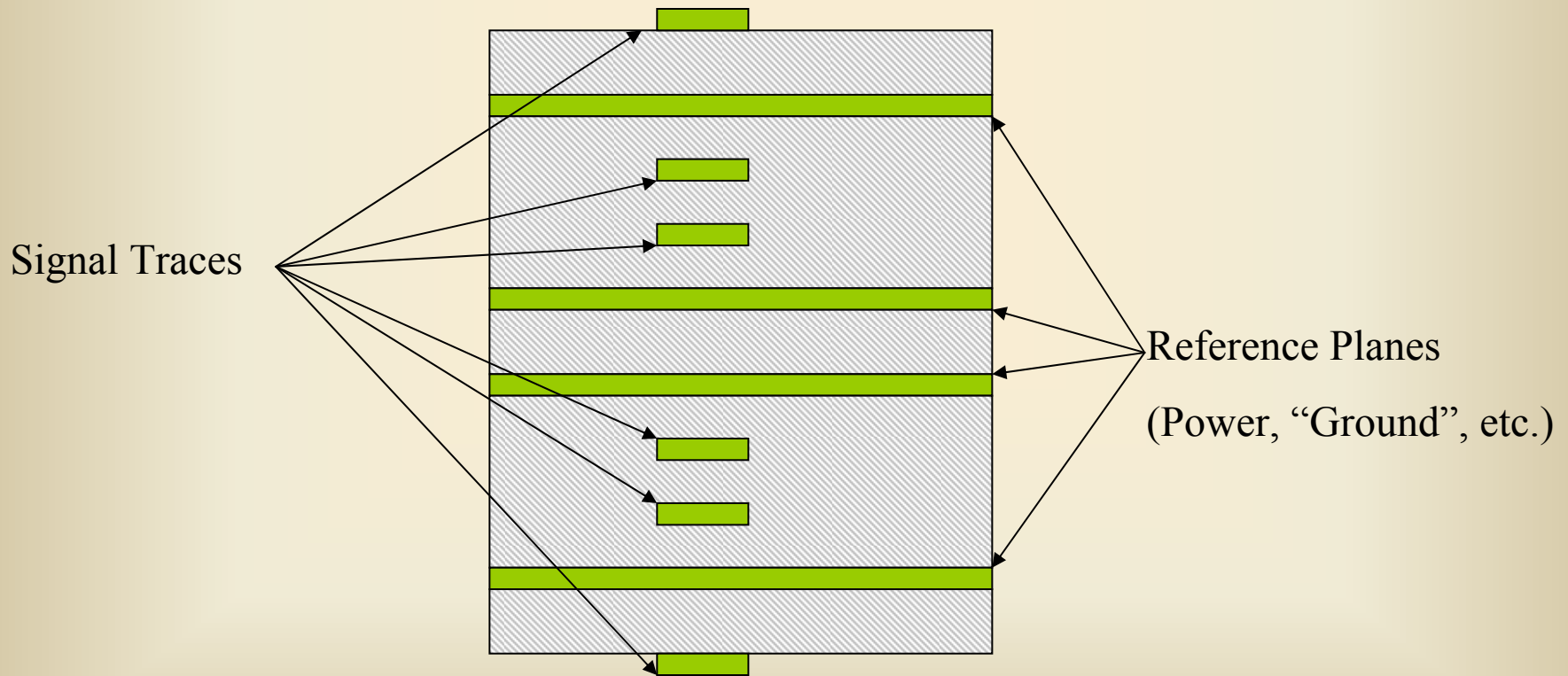
High Frequency Return Currents Take Path of Least Inductance



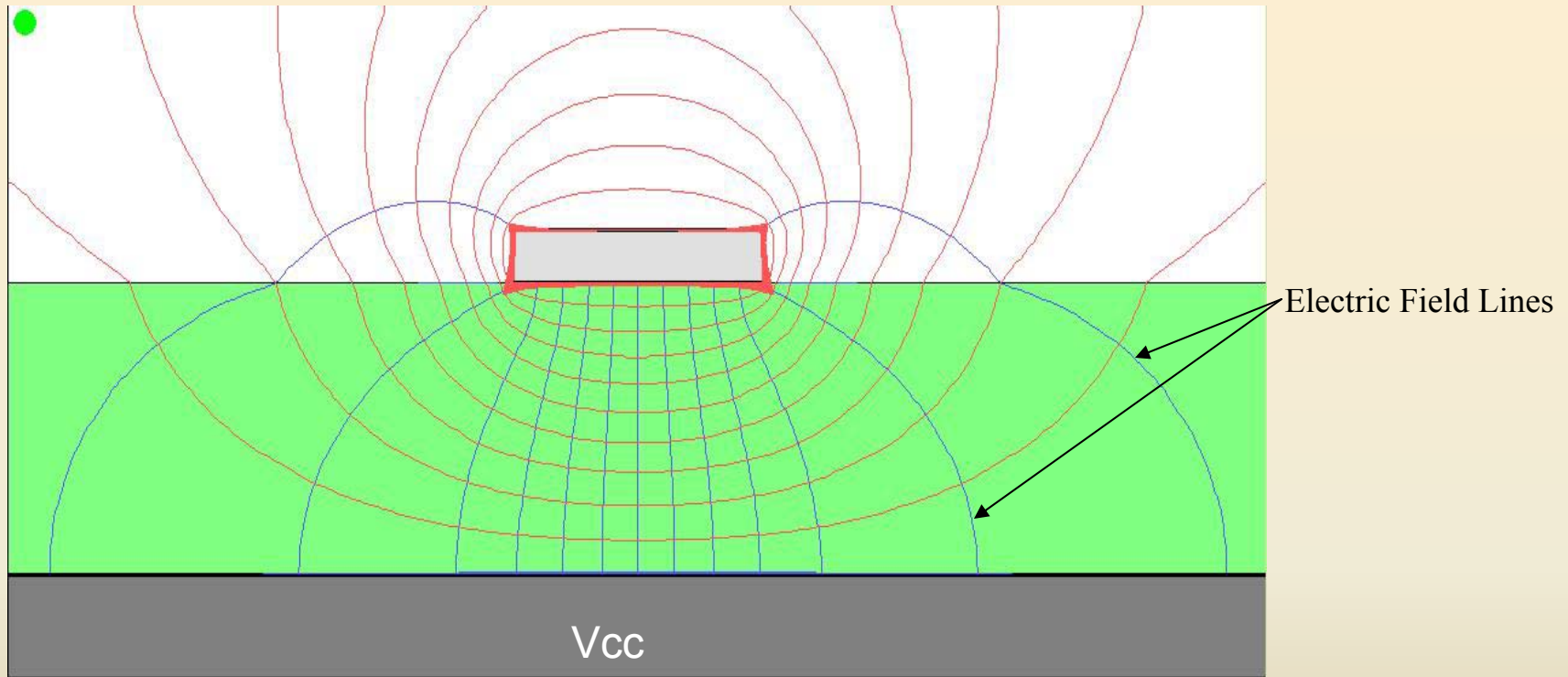
Traces/nets over a Reference Plane



Traces/nets and Reference Planes in Many Layer Board Stackup



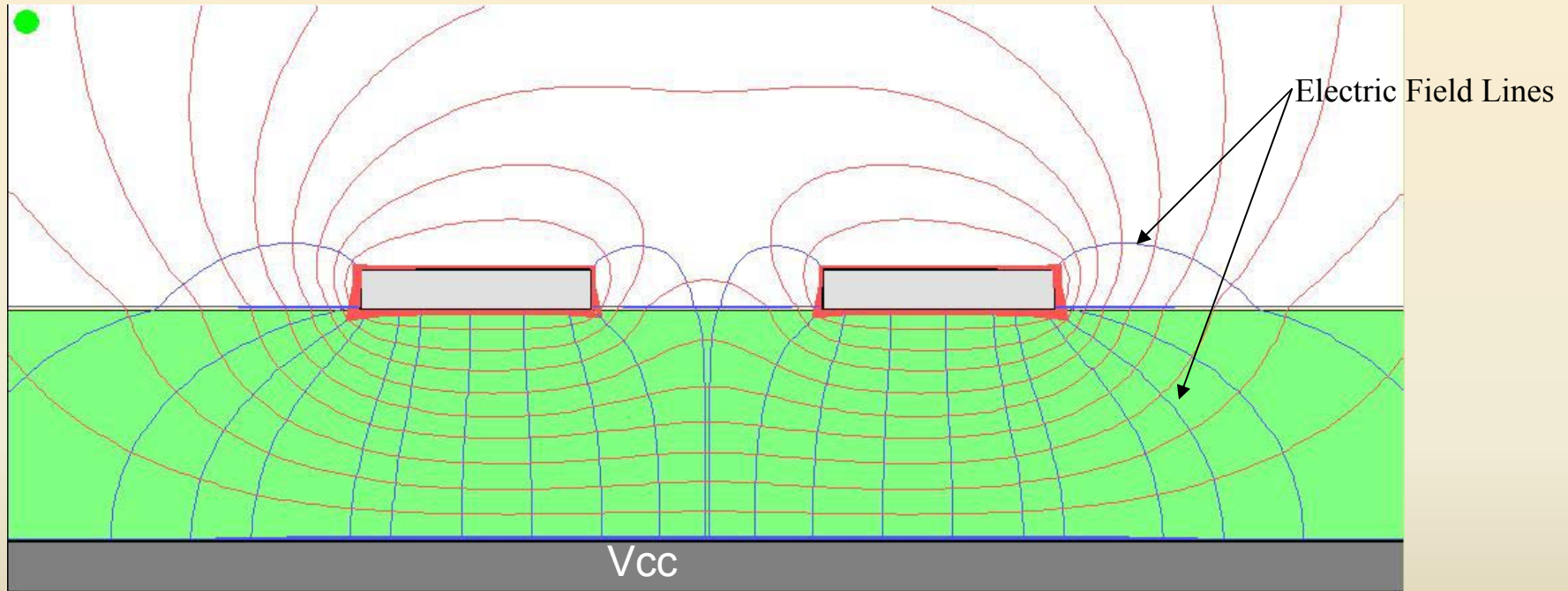
Microstrip Electric/Magnetic Field Lines (8mil wide trace, 8 mils above plane, 65 ohm)



Microstrip Electric/Magnetic Field Lines

Common Mode

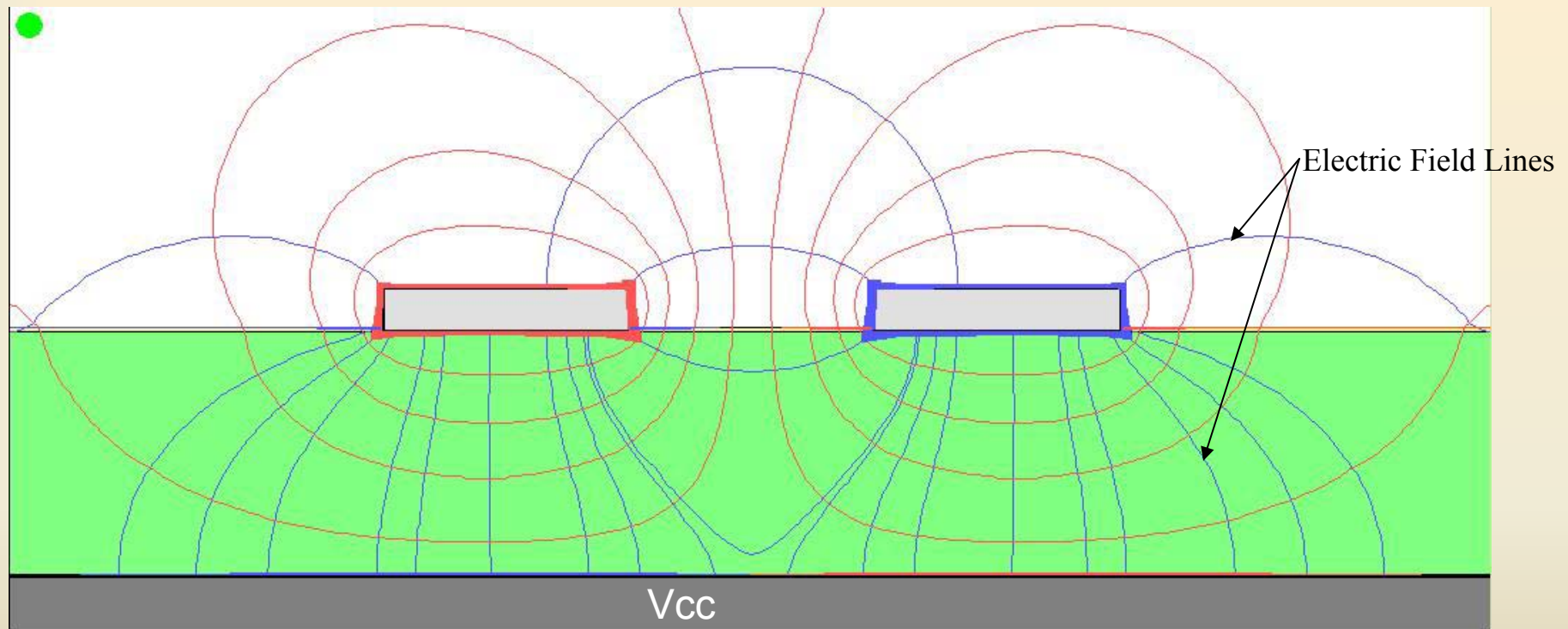
8 mil wide trace, 8 mils above plane, 65/115 ohm)



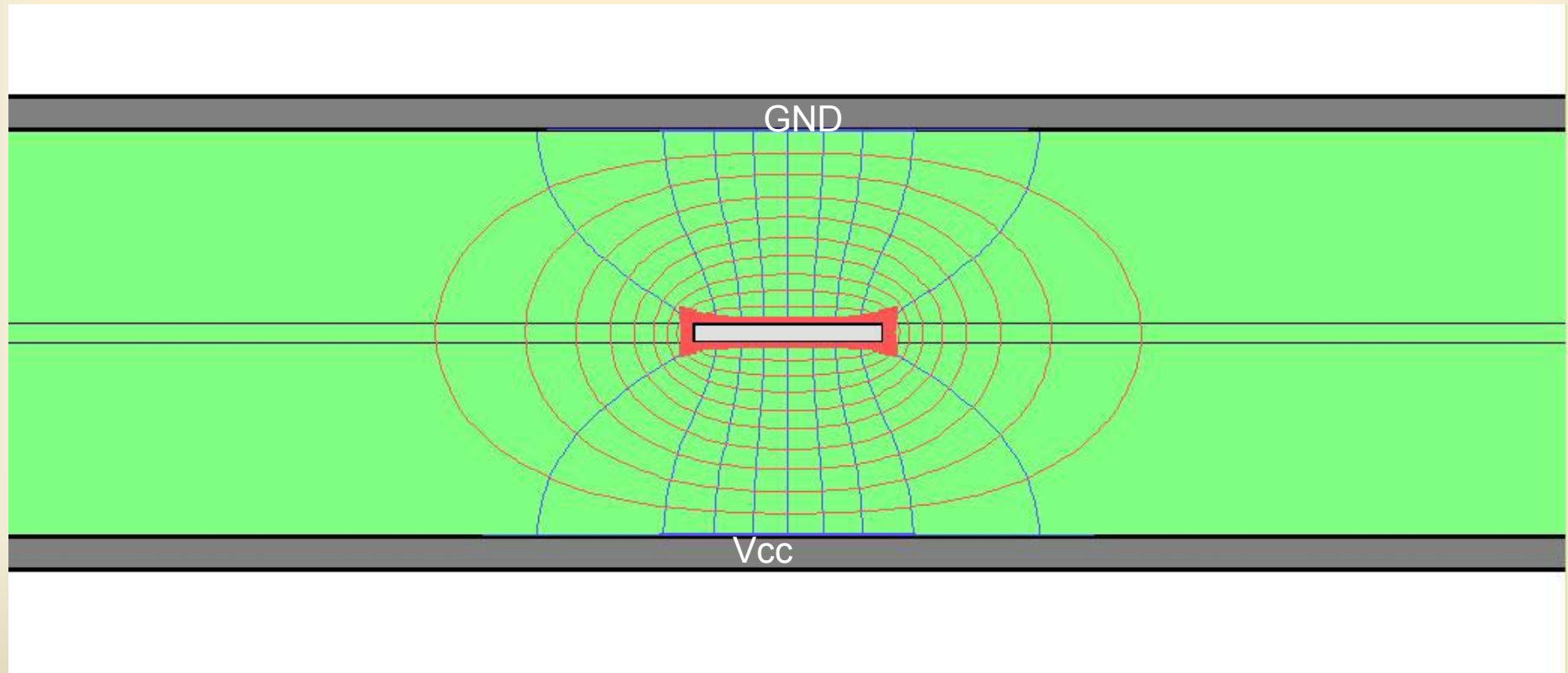
Microstrip Electric/Magnetic Field Lines

Differential Mode

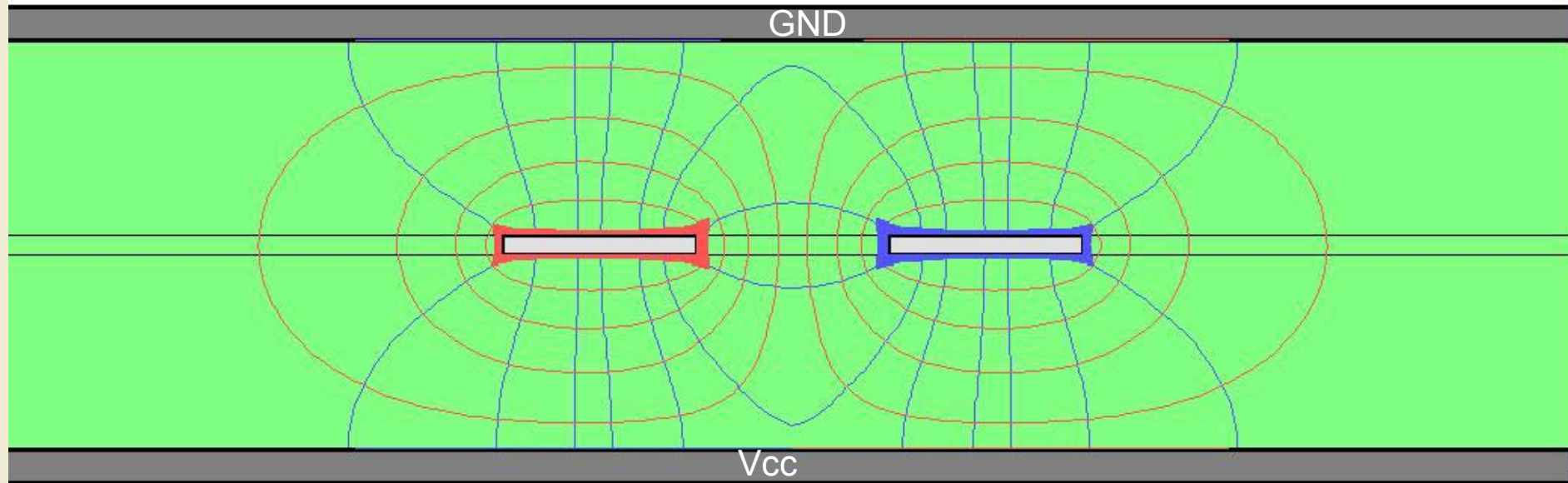
8 mil wide trace, 8 mils above plane, 65/115 ohm)



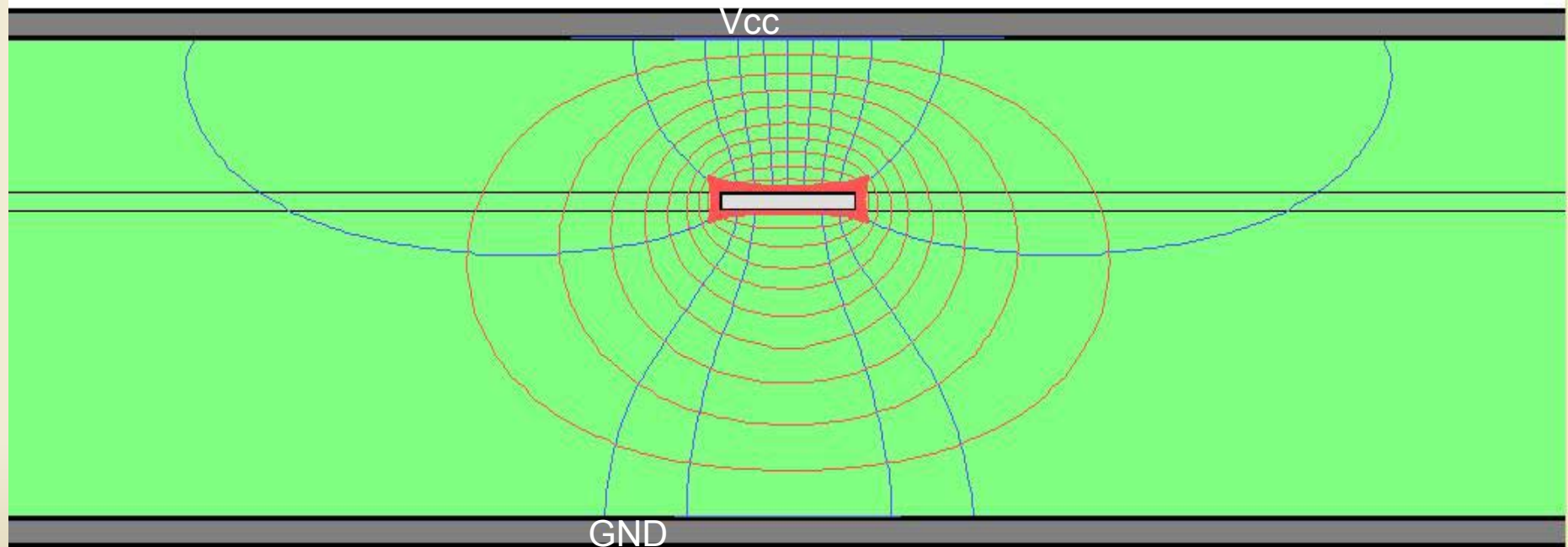
Electric/Magnetic Field Lines Symmetrical Stripline



Electric/Magnetic Field Lines Symmetrical Stripline (Differential)

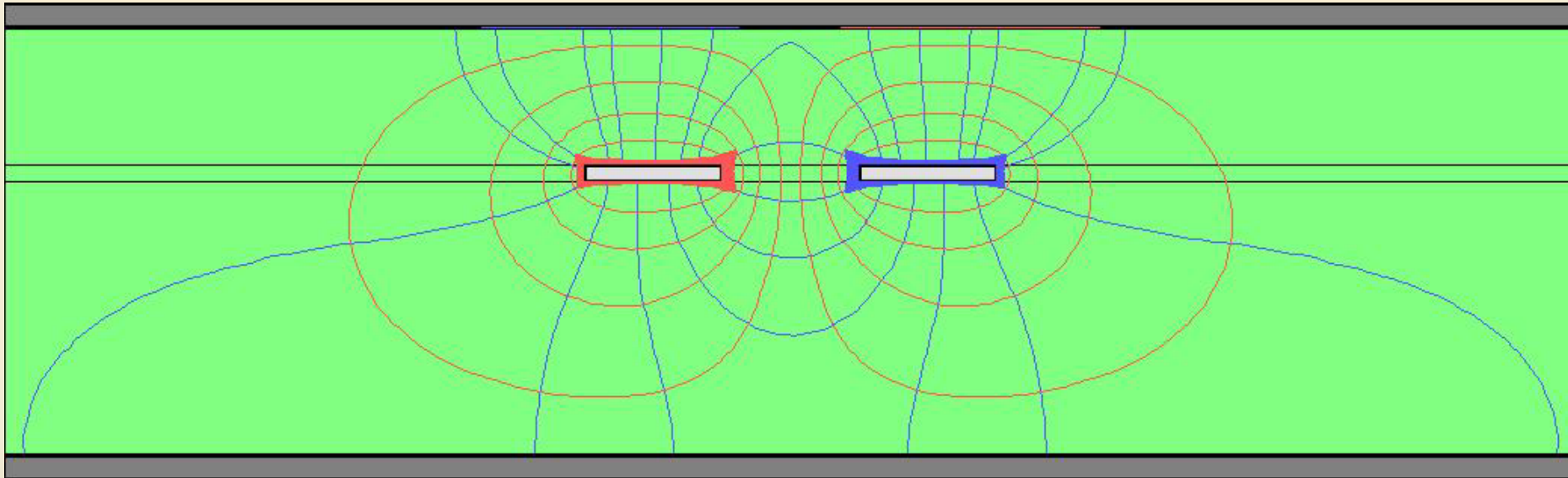


Electric/Magnetic Field Lines Asymmetrical Stripline



Electric/Magnetic Field Lines

Asymmetrical Stripline (Differential)



What About Pseudo-Differential Nets?

- So-called differential traces are NOT truly differential
 - Two complementary single-ended drivers
 - Relative to ‘ground’
 - Receiver is differential
 - Senses difference between two nets (independent of ‘ground’)
 - Provides good immunity to common mode noise
 - Good for signal quality/integrity

Pseudo-Differential Nets Current in Nearby Plane

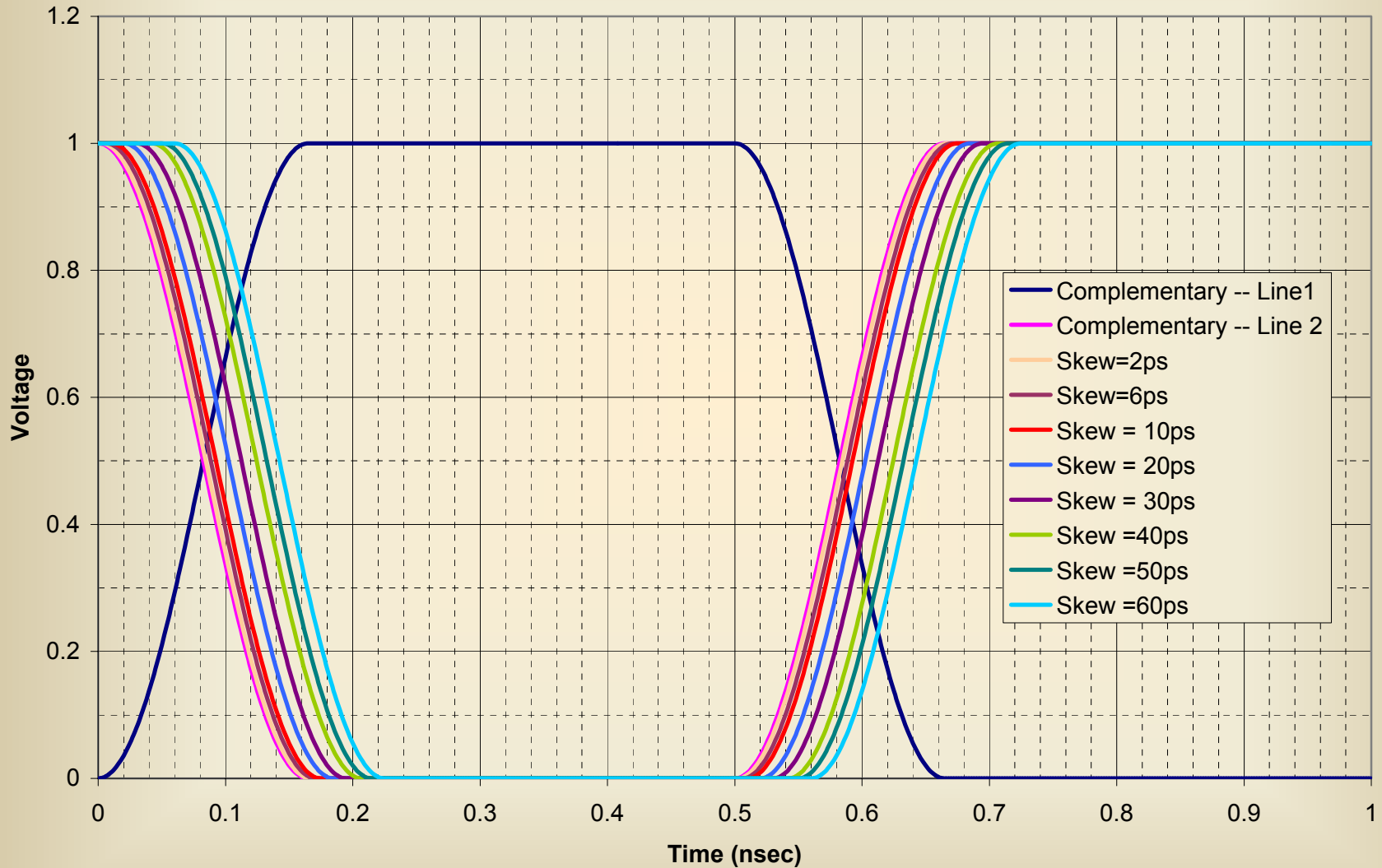
- Balanced/Differential currents have matching current in nearby plane
 - No issue for discontinuities
- Any unbalanced (common mode) currents have return currents in nearby plane that must return to source!
 - All normal concerns for single-ended nets apply!

Pseudo-Differential Nets

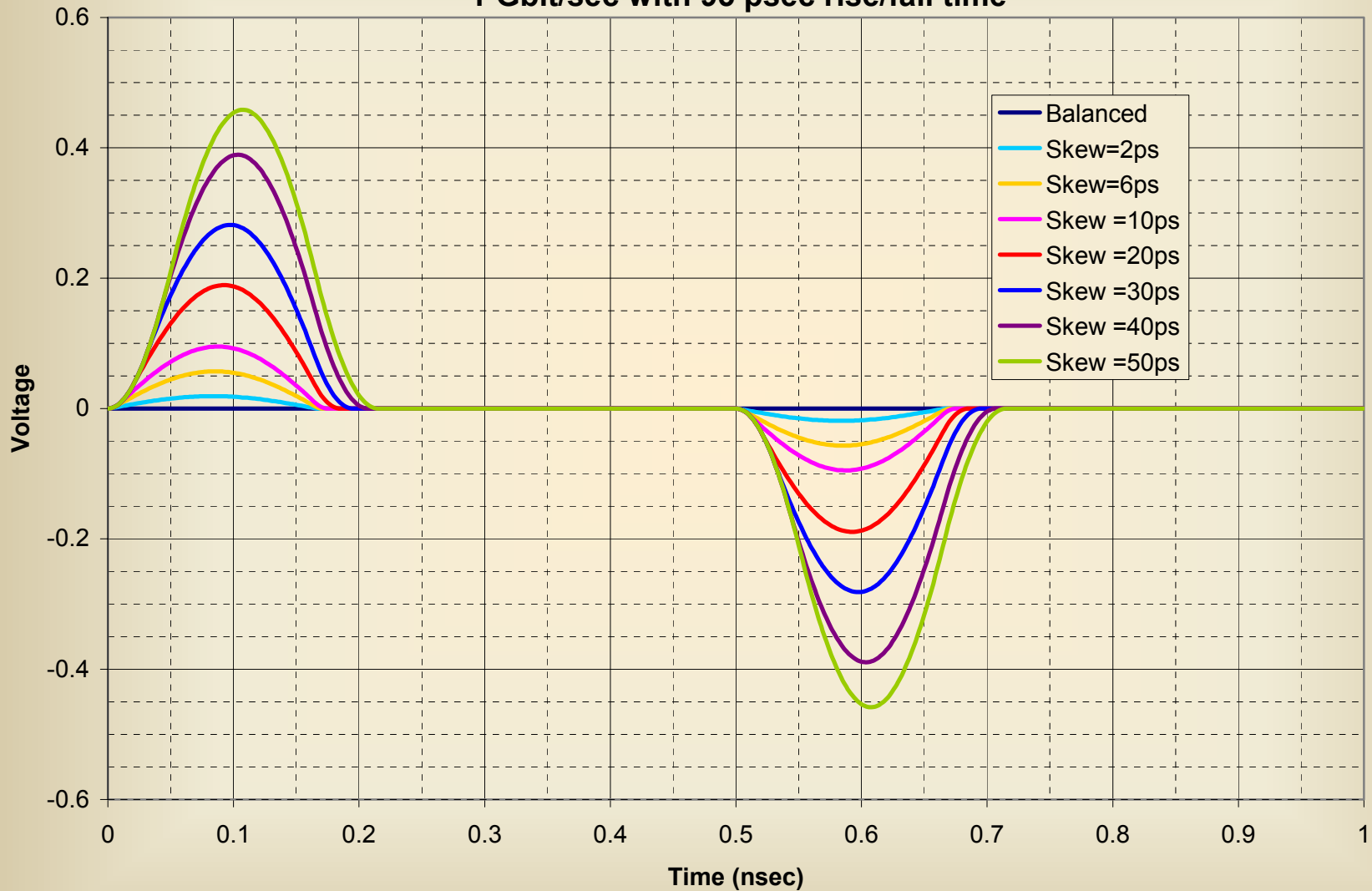
- Not really 'differential', since more closely coupled to nearby plane than each other
- Slew and rise/fall variation cause common mode currents!

Differential Voltage Pulse with Skew

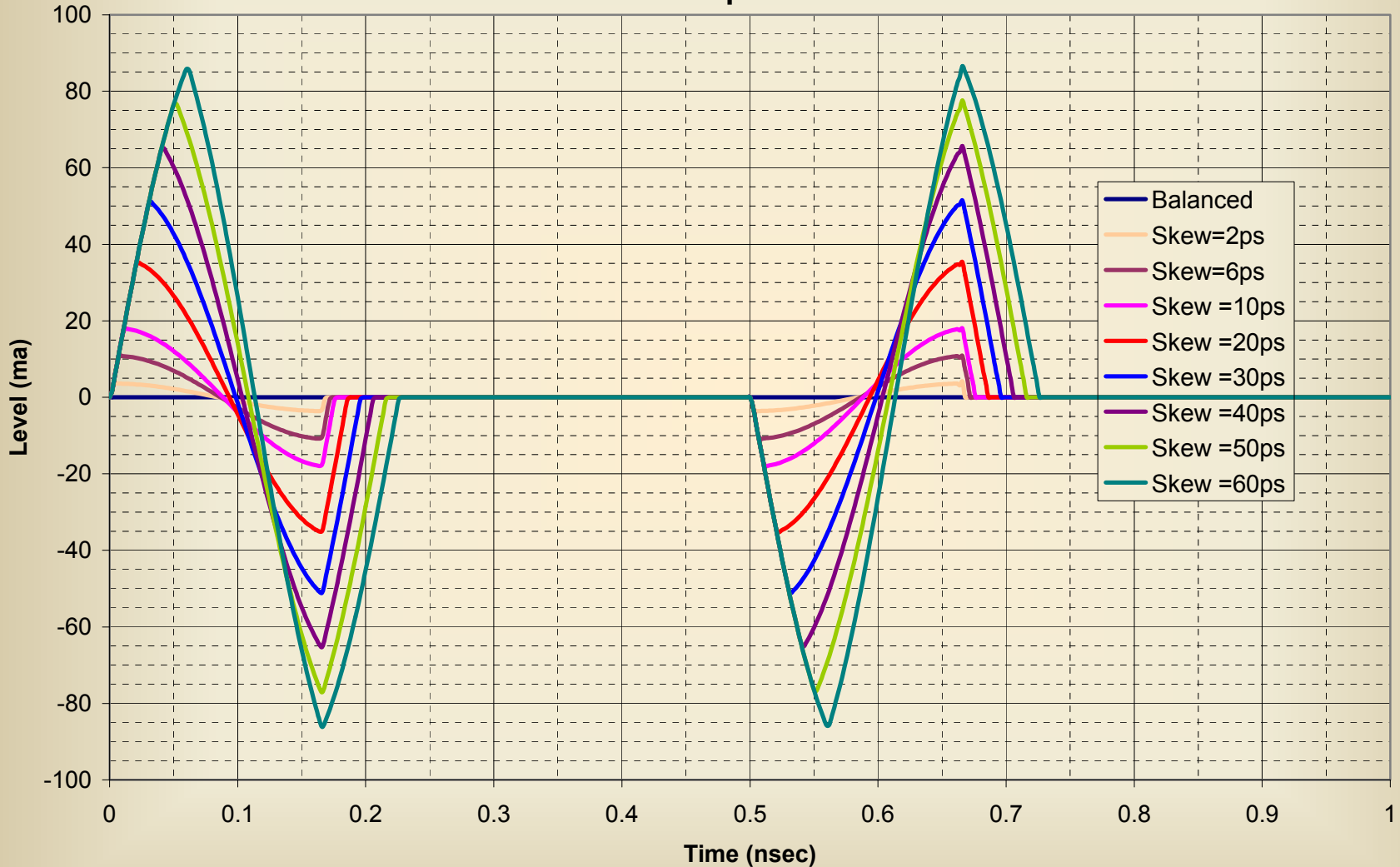
1 Gbit/sec with 95 psec rise/fall time



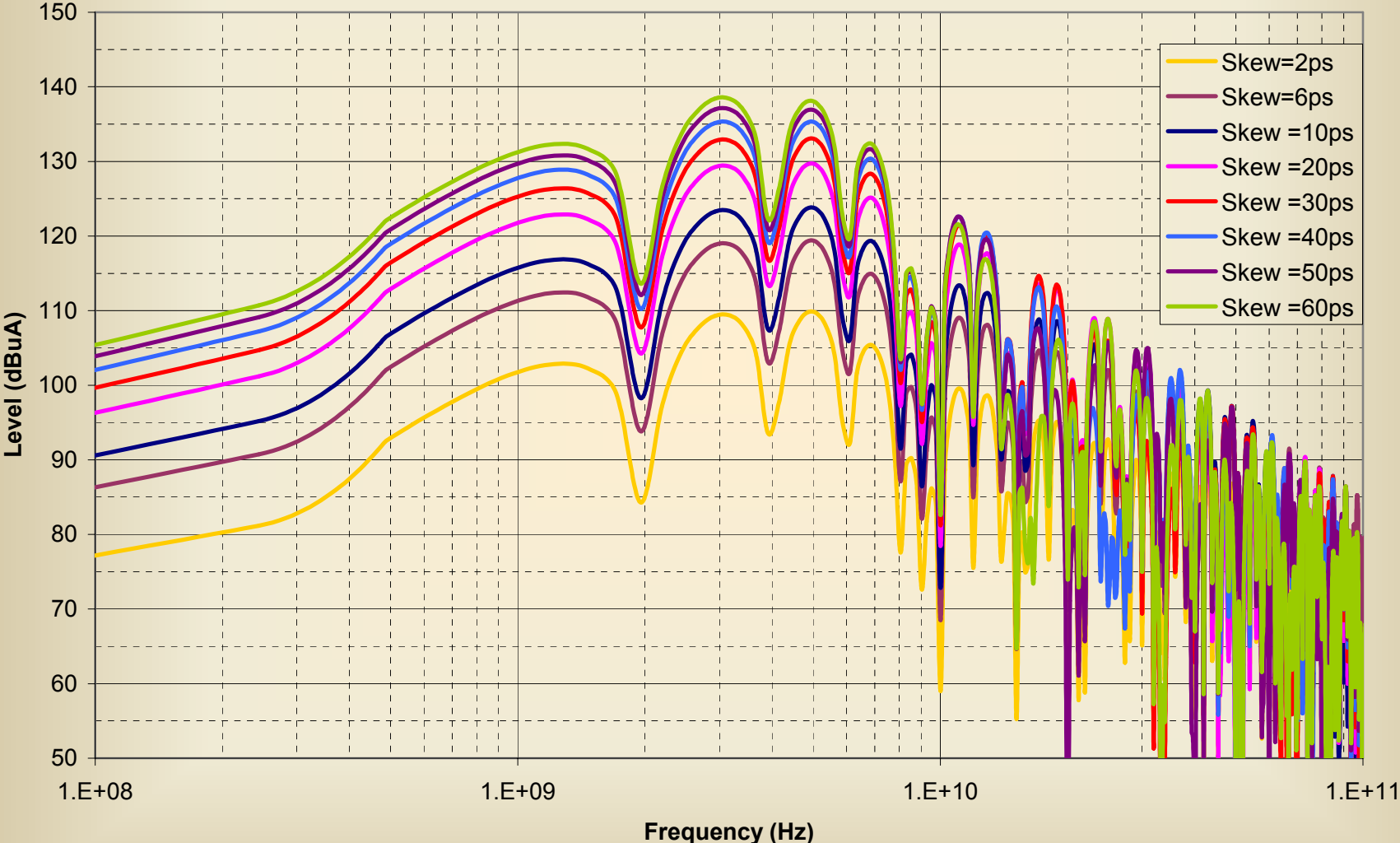
Common Mode Voltage From Differential Voltage Pulse with Skew 1 Gbit/sec with 95 psec rise/fall time



Common Mode Current From Differential Voltage Pulse with Skew 1 Gbit/sec with 95 psec Rise/fall Time

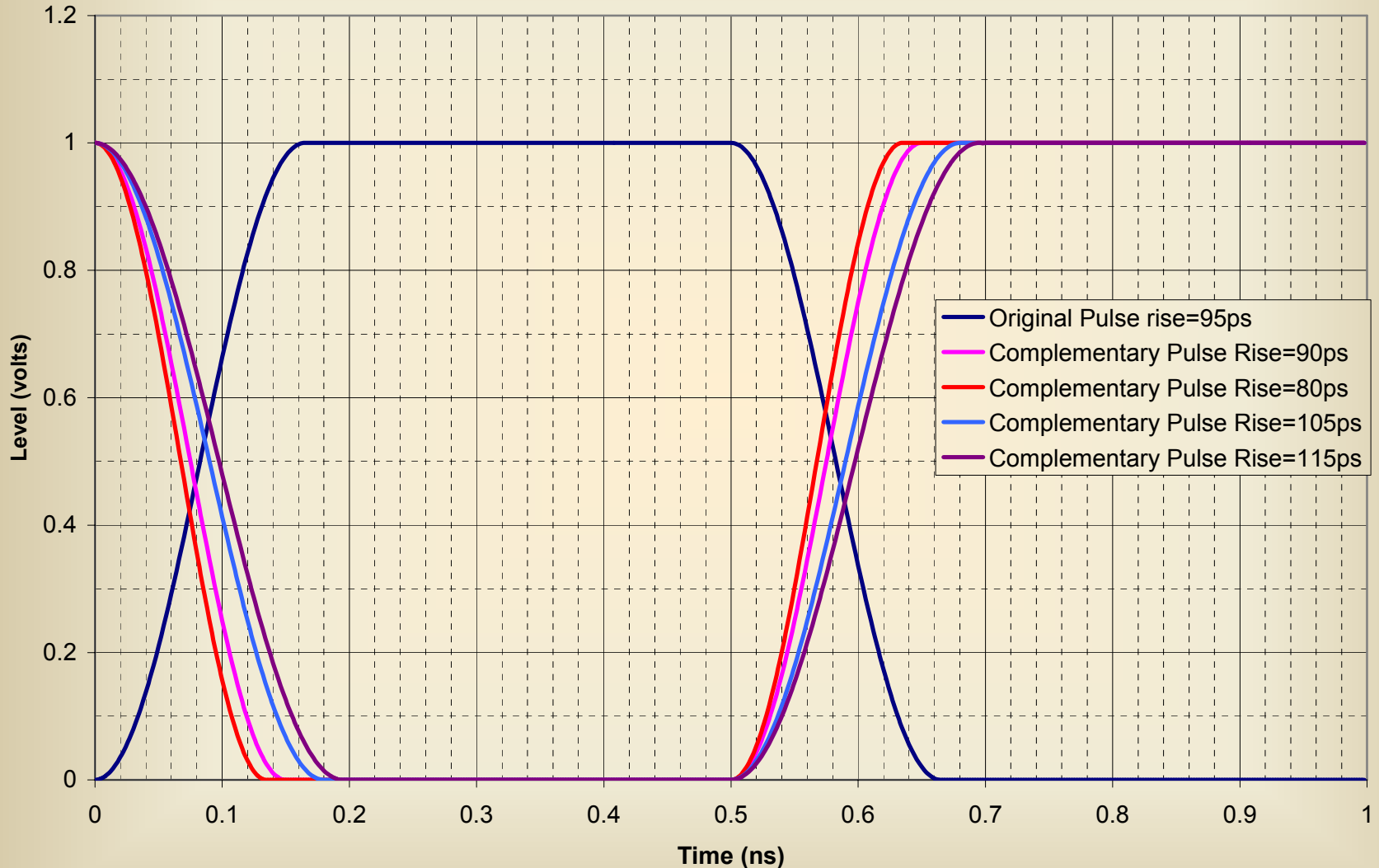


**Common Mode Current
From Differential Voltage Pulse with Skew
1 Gbit/sec with 95 psec Rise/fall Time**

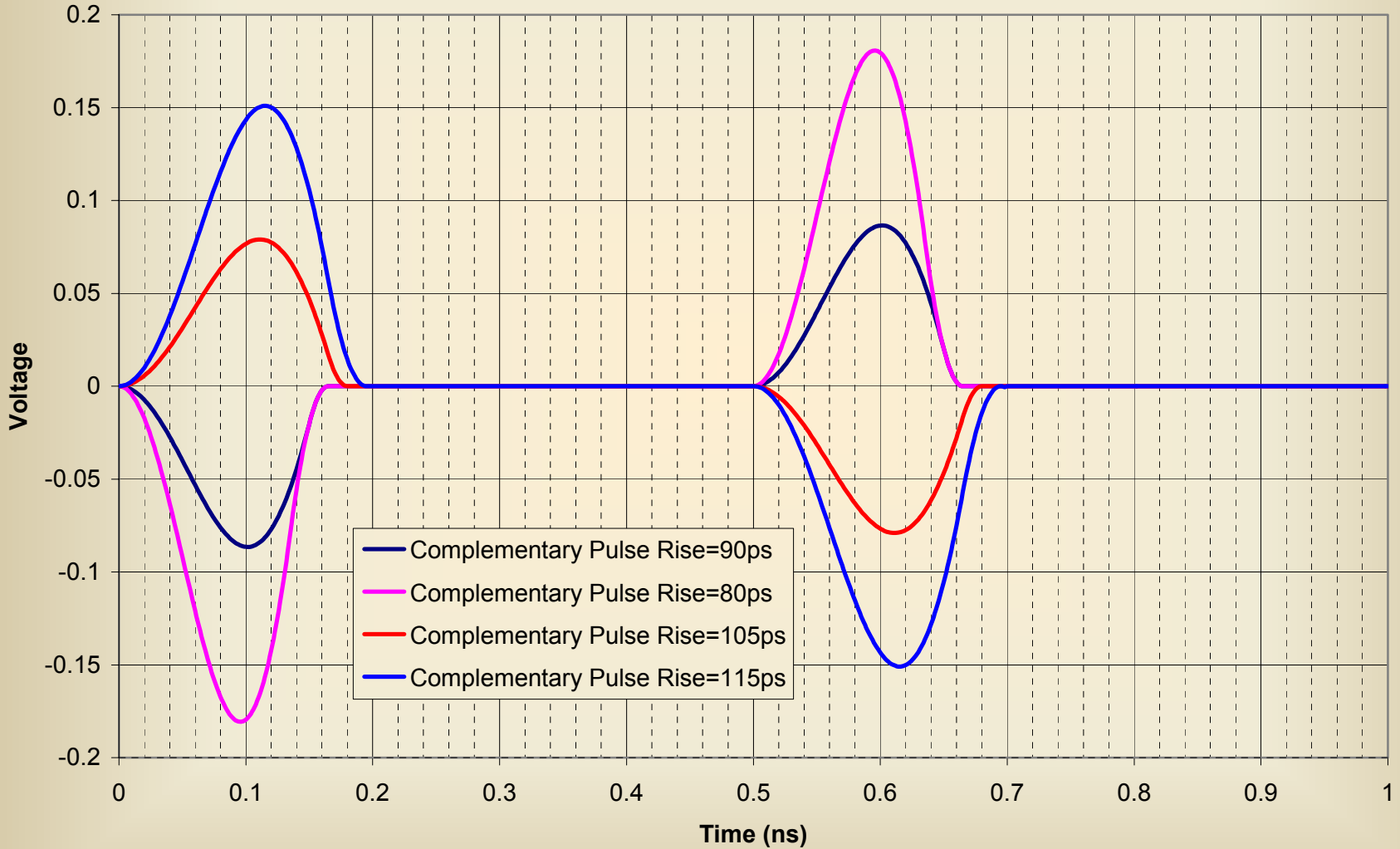


Differential Voltage Pulse with Rise/Fall Variation/Unbalance

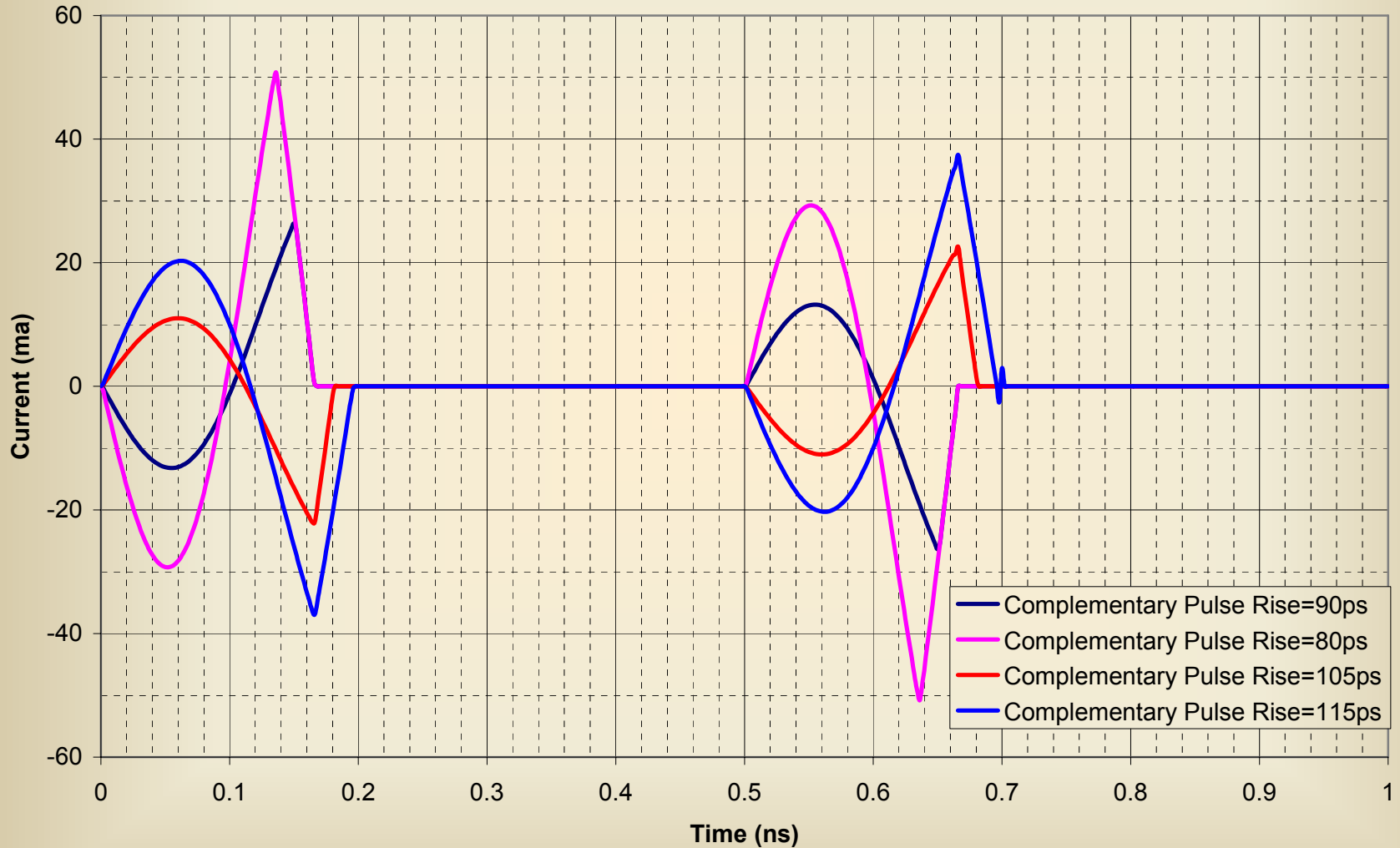
1 Gbit/sec with 95 psec Nominal Rise/Fall Time



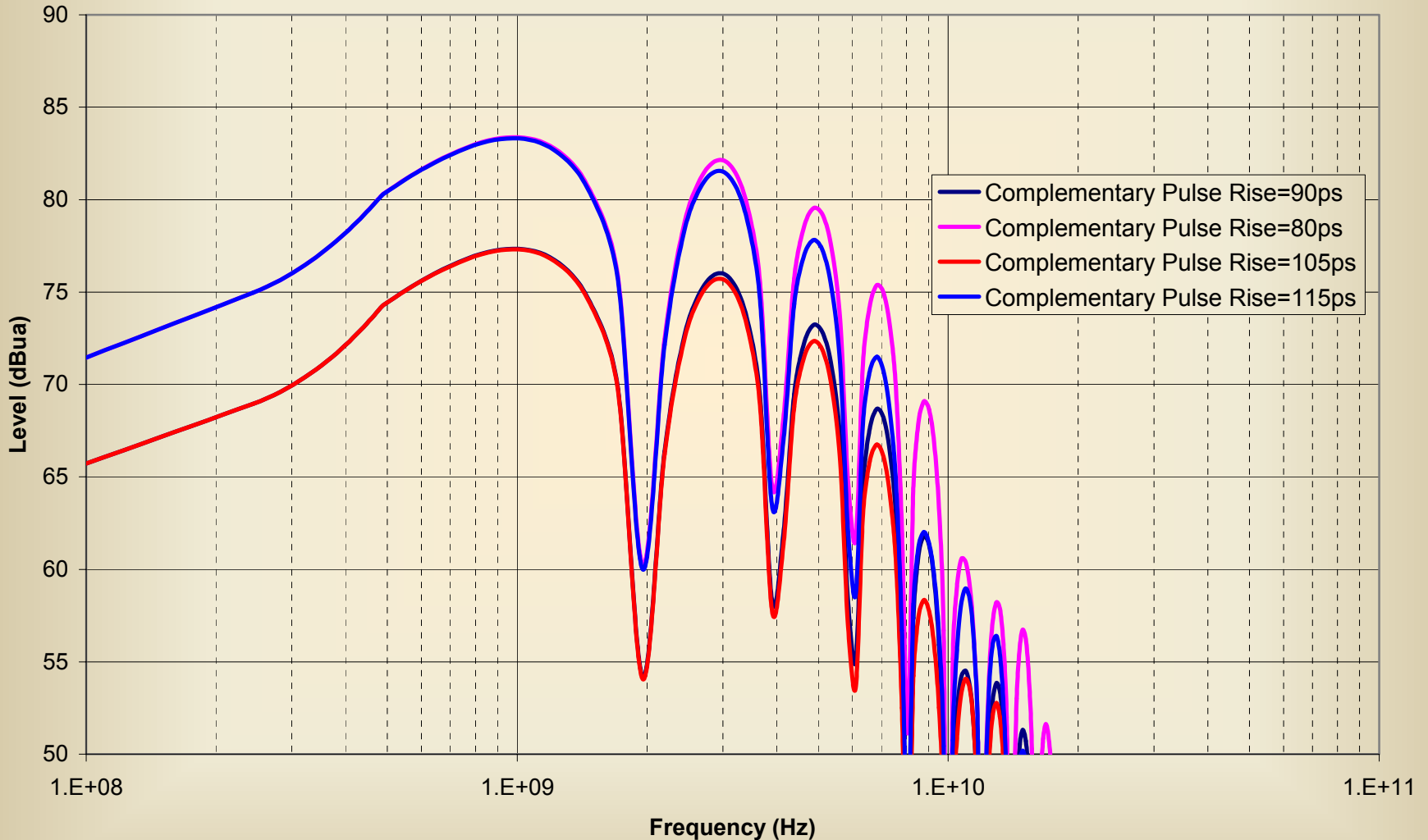
Common Mode Voltage From Differential Voltage Pulse with Various Rise/Fall Unbalance 1 Gbit/sec with 95 psec Nominal Rise/Fall Time



Common Mode Current From Differential Voltage Pulse with Various Rise/Fall Unbalance 1 Gbit/sec with 95 psec Nominal Rise/fall Time



Common Mode Current From Differential Voltage Pulse with Various Rise/Fall Unbalance 1 Gbit/sec with Nominal 95 psec Rise/fall Time

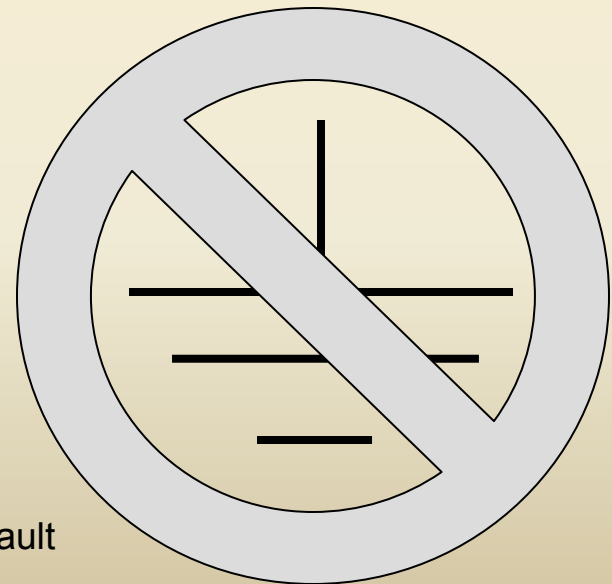


Pseudo-Differential Net Summary

- Small amounts of skew can cause significant common mode current
- Small amount of rise/fall time deviation can cause significant amount of common mode current
- Discontinuities (vias, crossing split planes, etc) and convert significant amount of differential current into common mode current

Return Current vs.. “Ground”

- For high frequency signals, “Ground” is a concept that does not exist
- The important question is “where does the return current flow?”



Referencing Nets

(Where does the Return Current Flow??)

- Microstrip/Stripline across split in reference plane
- Microstrip/Stripline through via (change reference planes)
- Mother/Daughter card

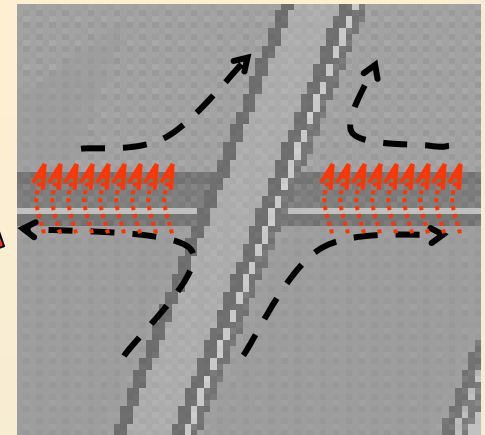
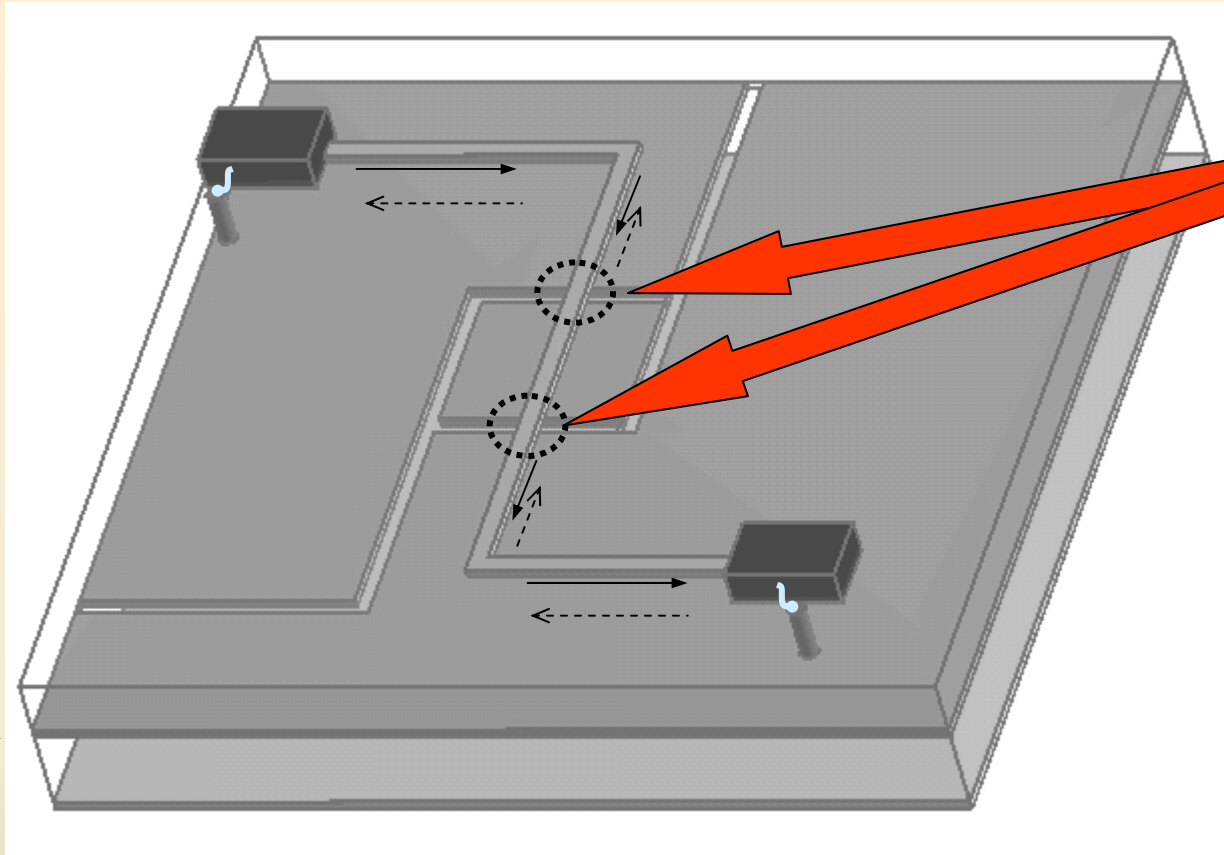
Microstrip/Stripline Across Split in Reference Plane

- Don't Cross Splits with Critical Signals!!!
 - Bad practice
 - Stitching capacitor required across split to allow return current flow
 - must be close to crossing
 - must have low inductance
 - limited frequency effect --- due to inductance
 - Major source of Common Mode current!

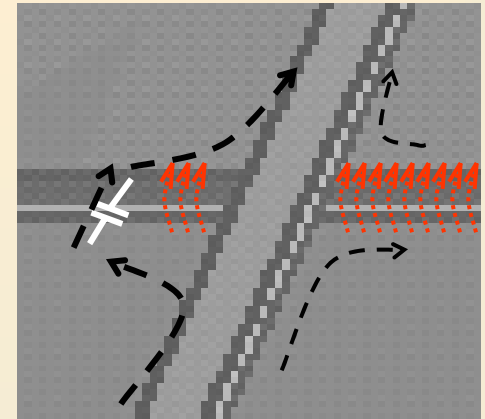
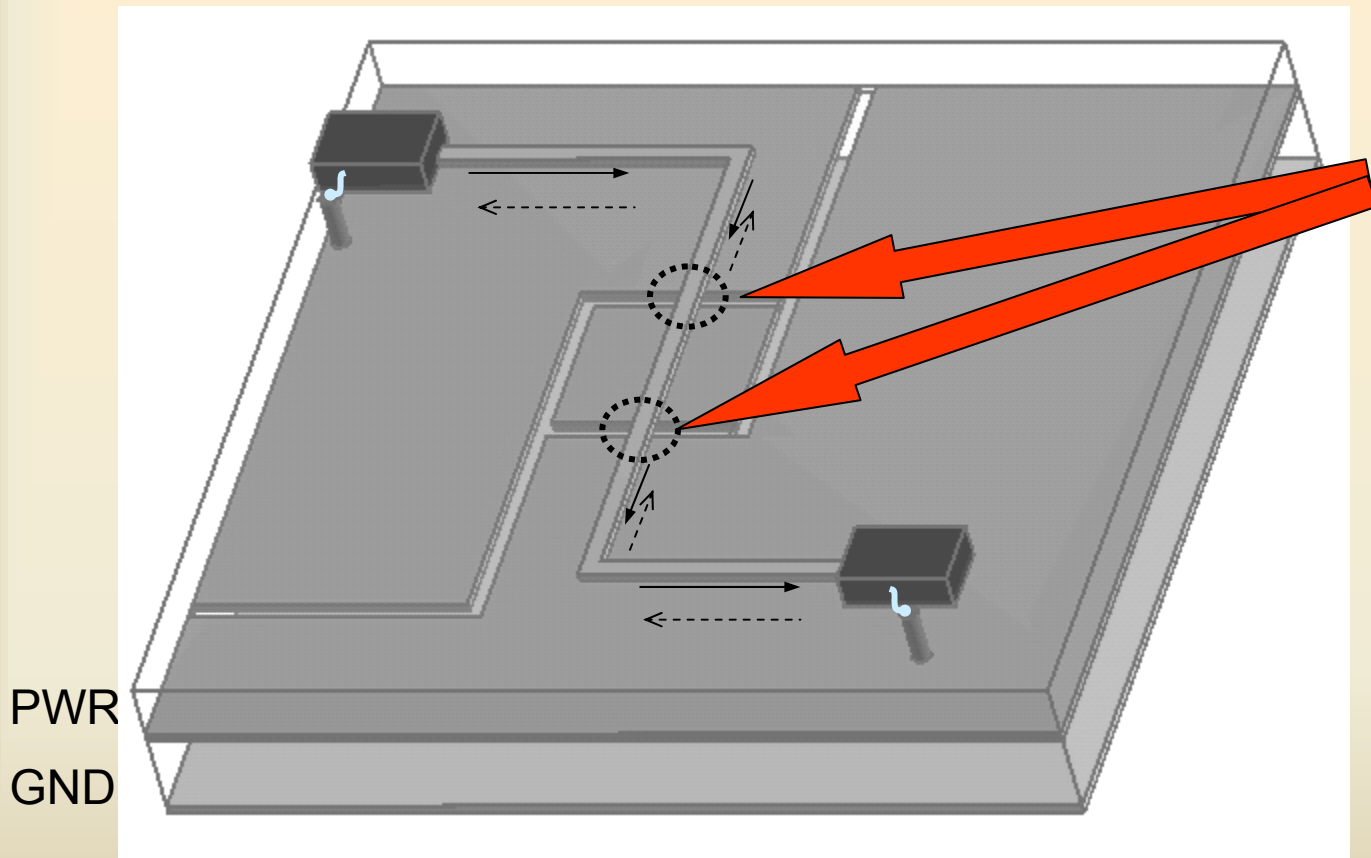
Splits in Reference Plane

- Power planes often have splits
- Return current path interrupted
- Consider spectrum of clock signal
- Consider stitching capacitor impedance
- High frequency harmonics not returned directly

Split Reference Plane Example



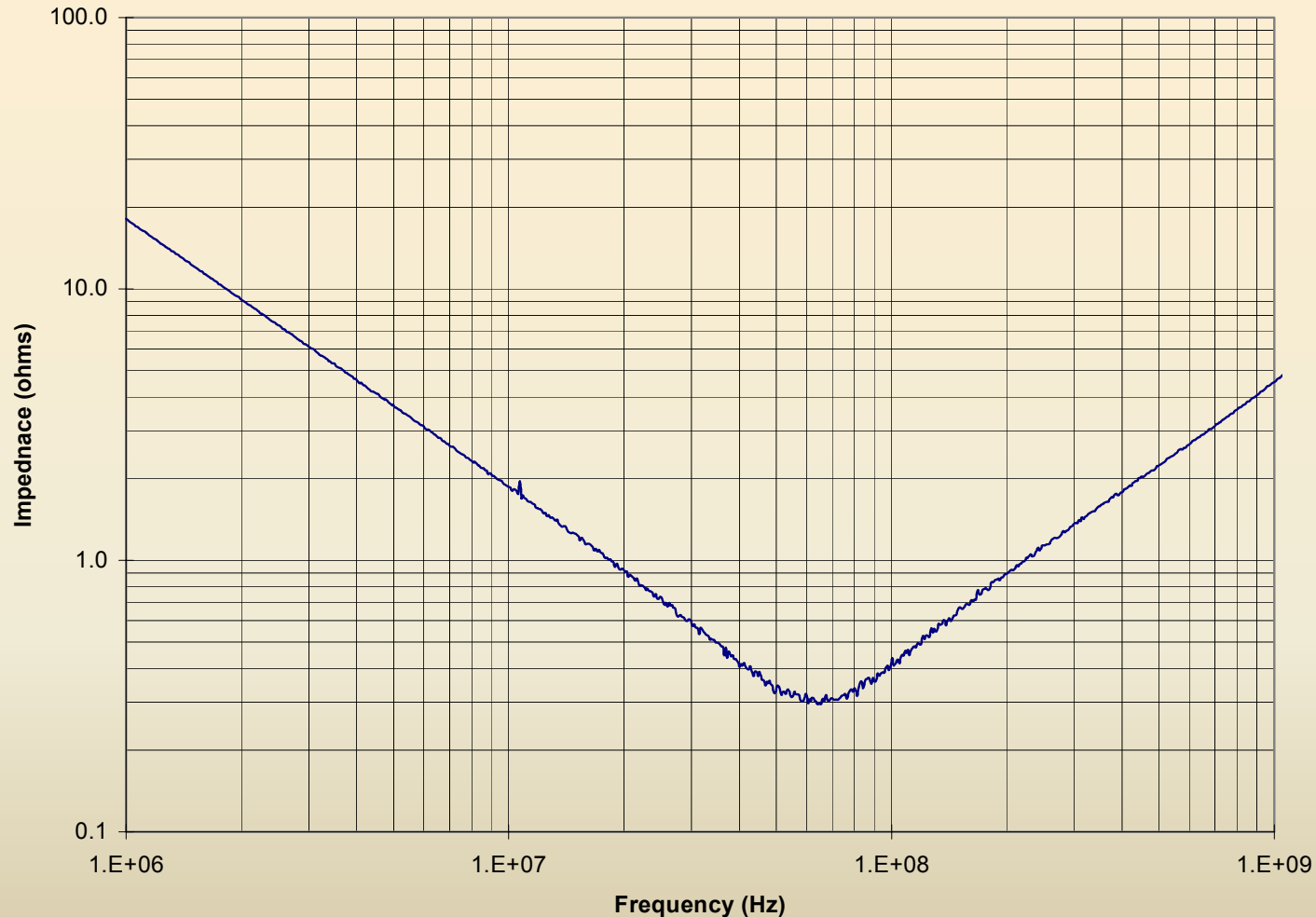
Split Reference Plane Example With Stitching Capacitors



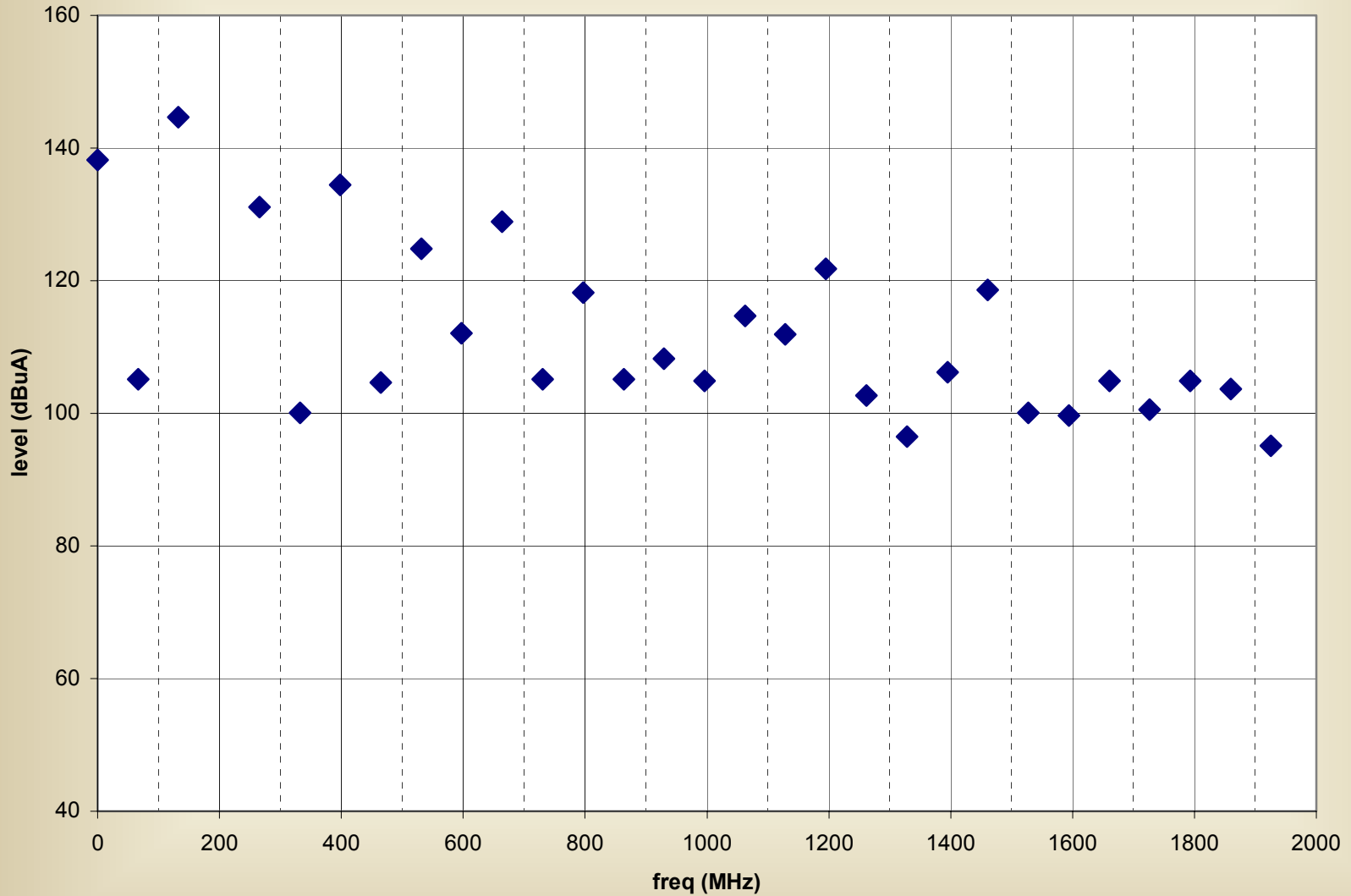
**Stitching Capacitors
Allow Return
current to Cross
Splits ???**

Capacitor Impedance

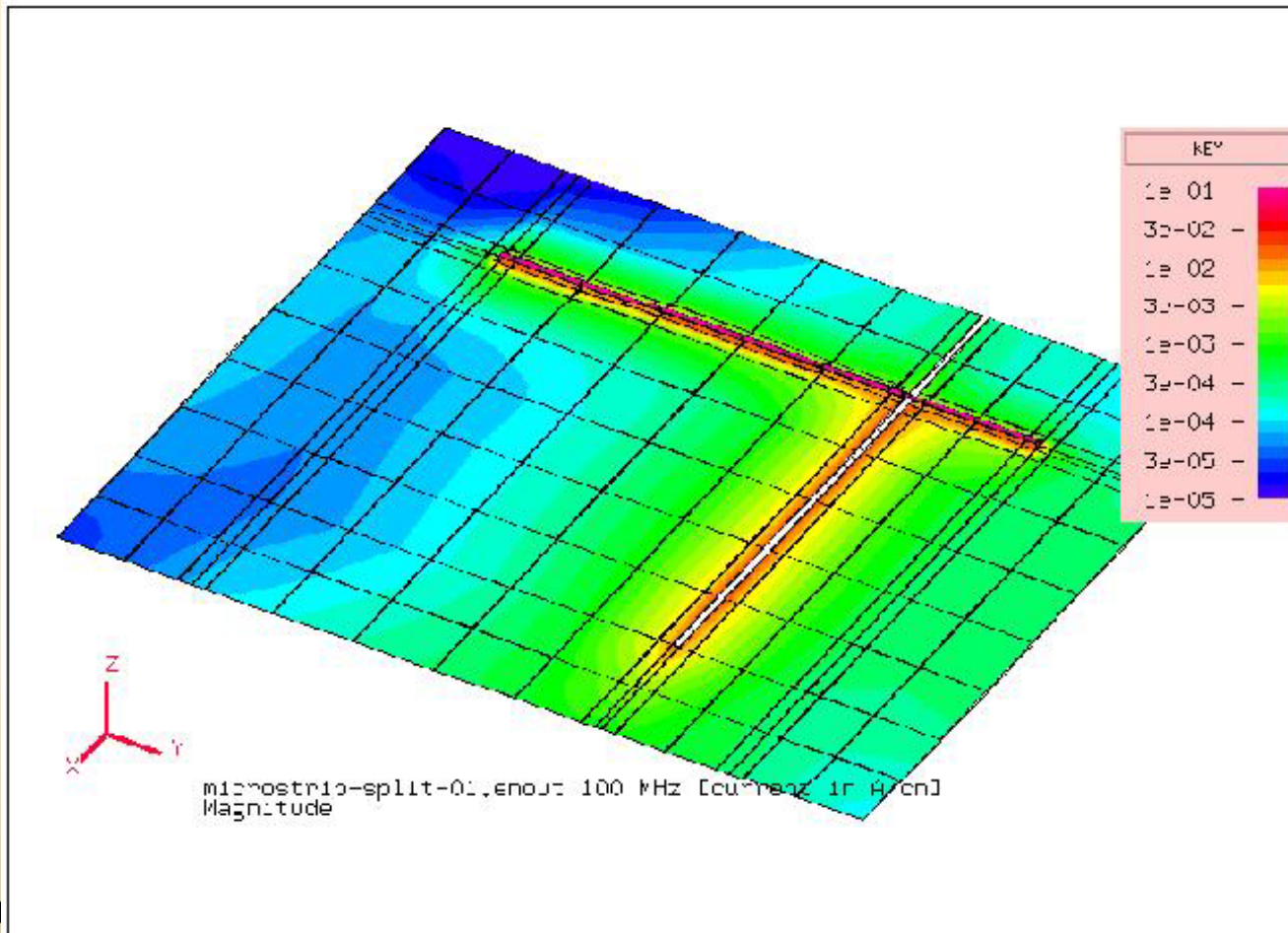
Measured Impedance of .01 uf Capacitor



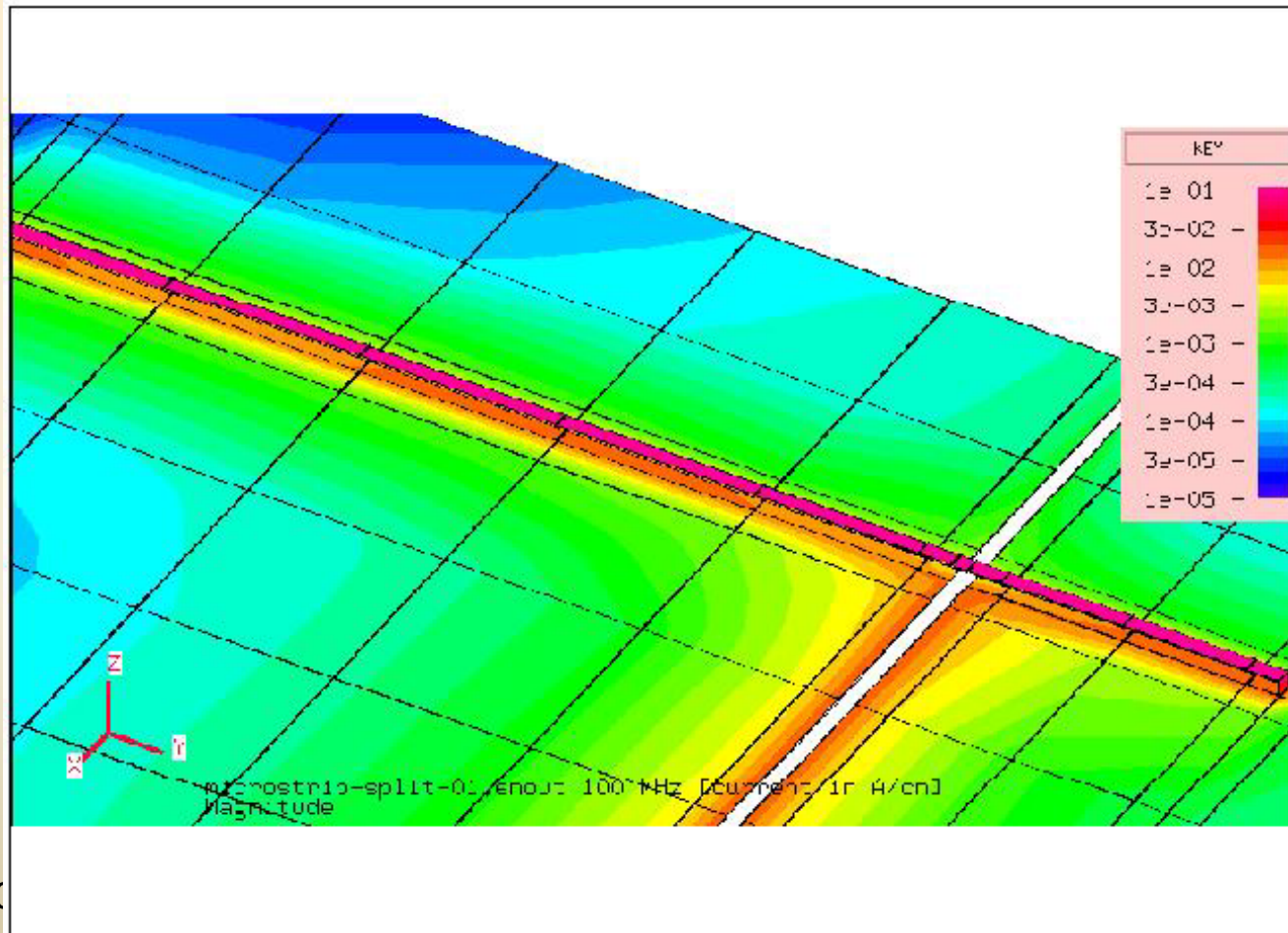
Frequency Domain Amplitude of Intentional Current Harmonic Amplitude From Clock Net



MoM Microstrip Model Current Distribution Example



MoM Microstrip Model Current Distribution Example

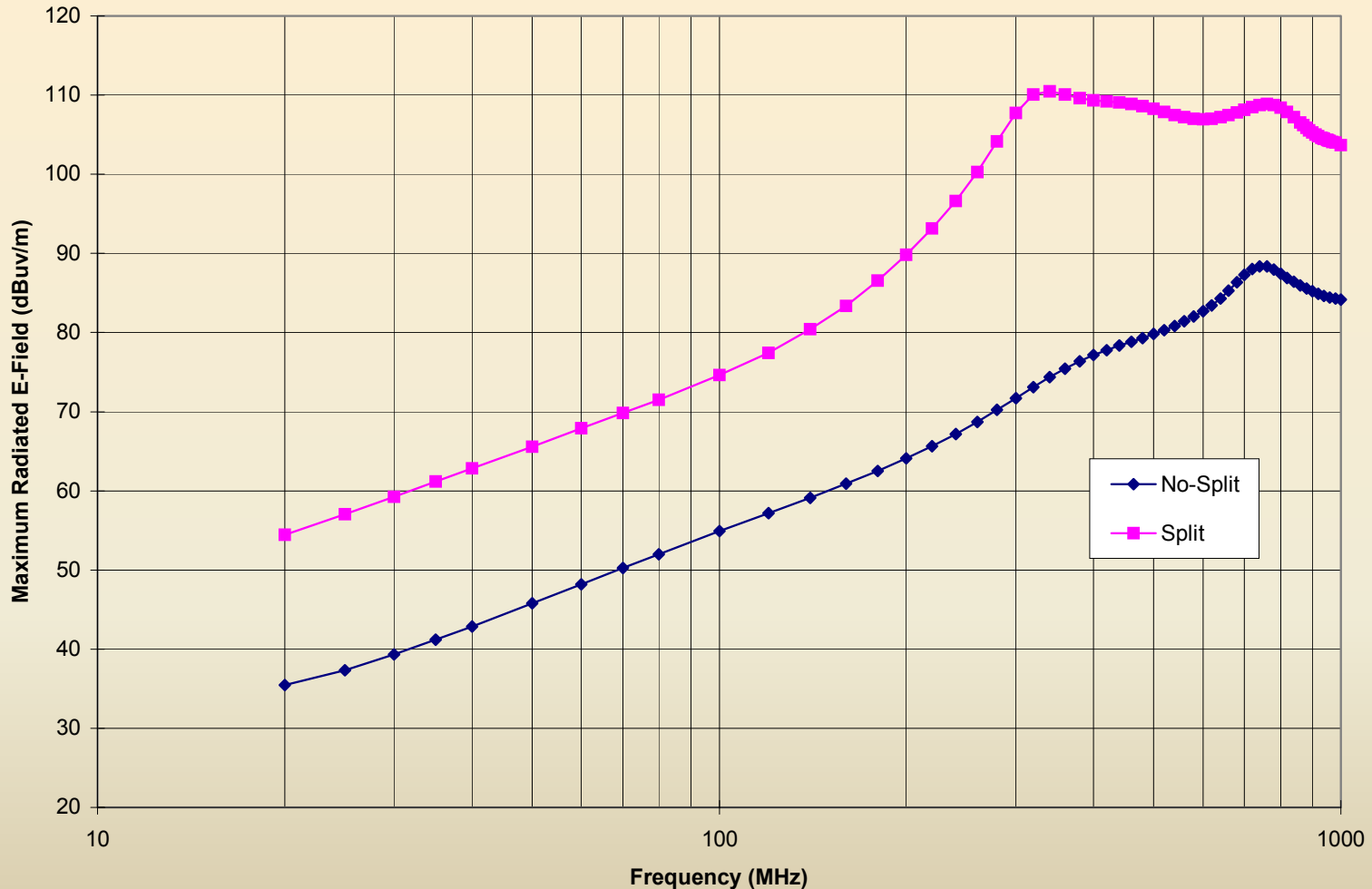


Emissions From Board

- Far field emissions not important unless it is an unshielded product
- Near field emissions above board **ARE** important
- Example of emissions from board with critical net crossing split reference plane

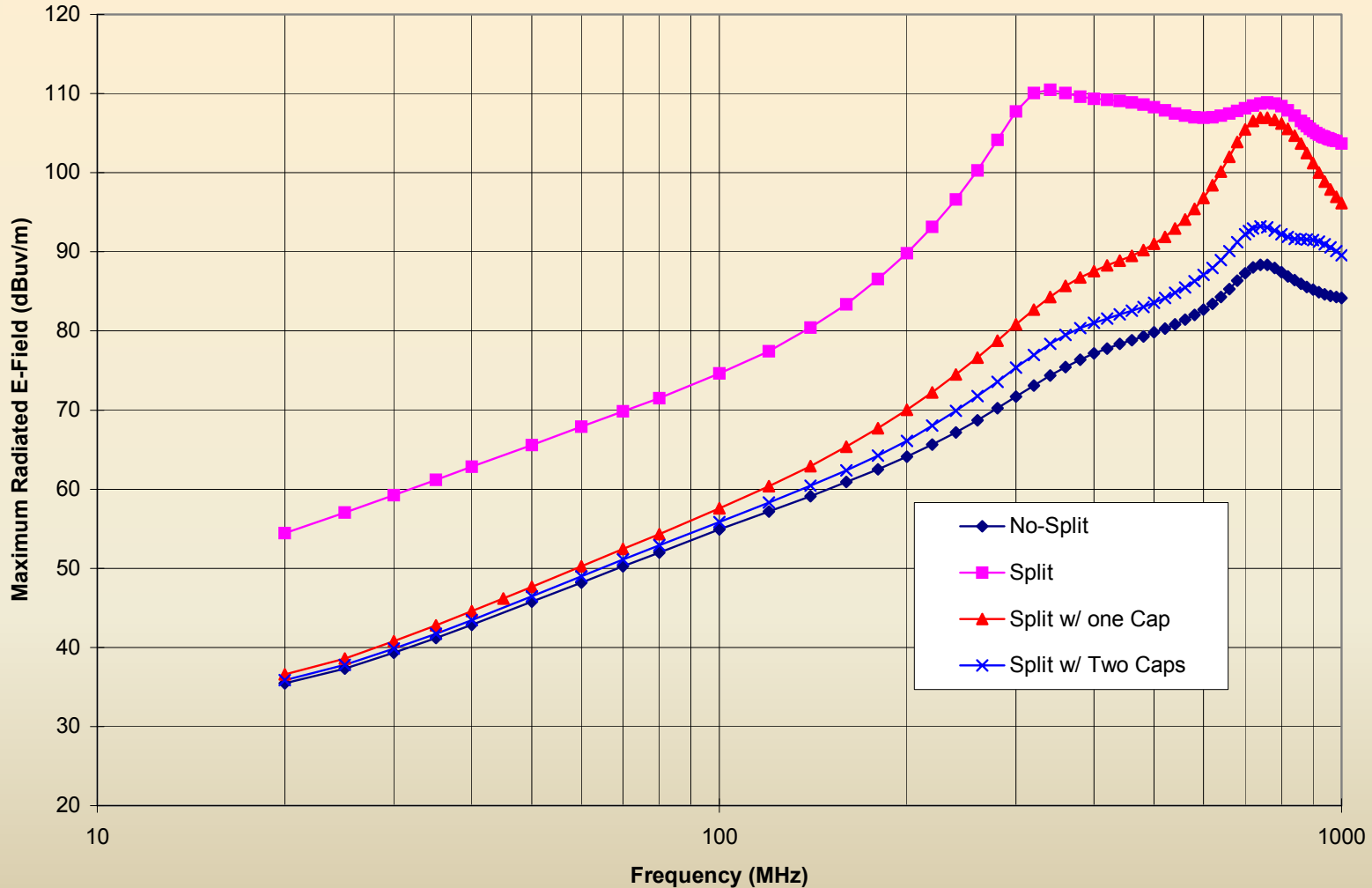
Near Field Radiation from Microstrip on Board with Split in Reference Plane

Comparison of Maximum Radiated E-Field for Microstrip With and without Split Ground Reference Plane



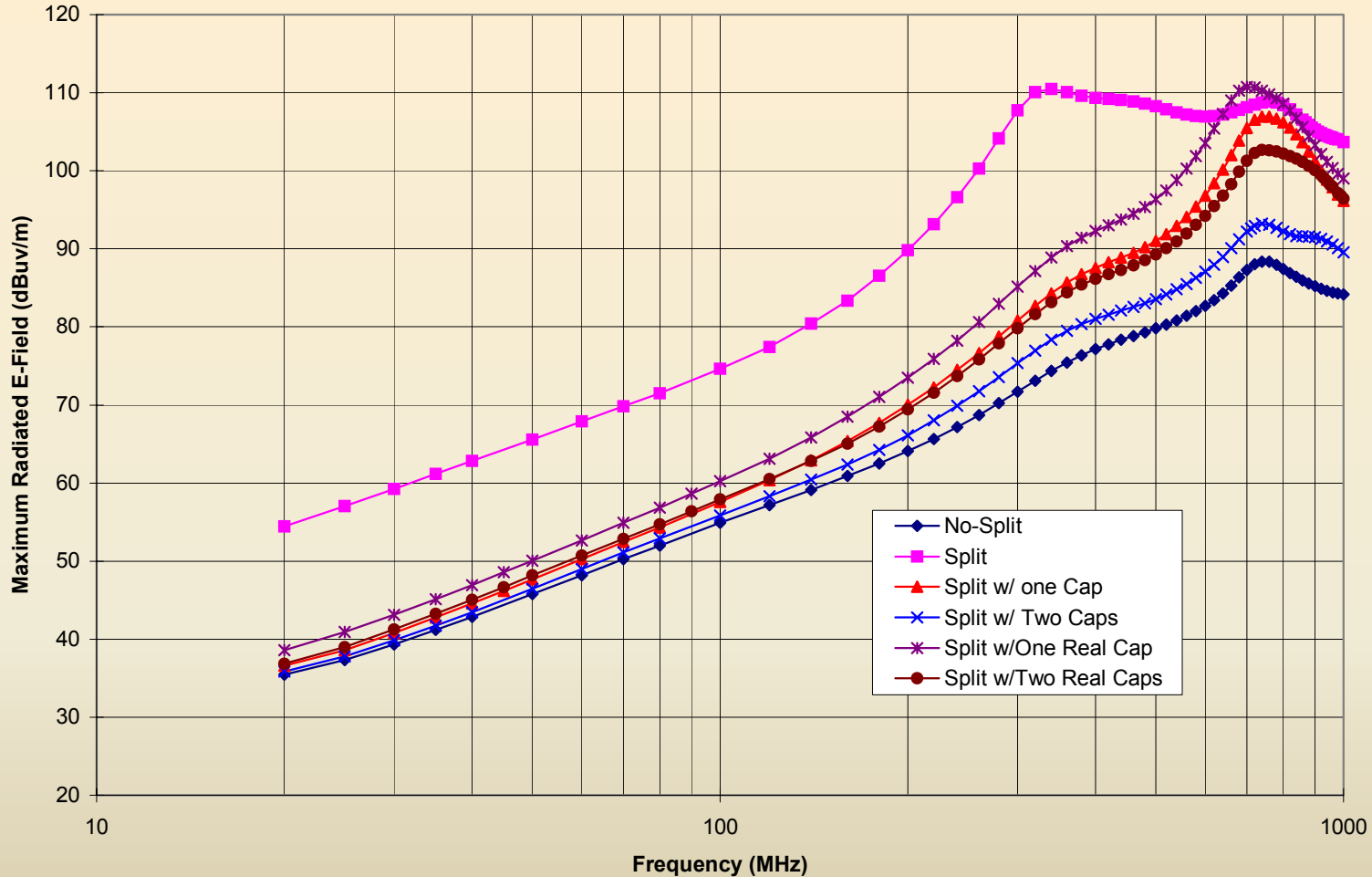
With “Perfectly Connected” Stitching Capacitors Across Split

Comparison of Maximum Radiated E-Field for Microstrip
With and without Split Ground Reference Plane and Stching Capacitors

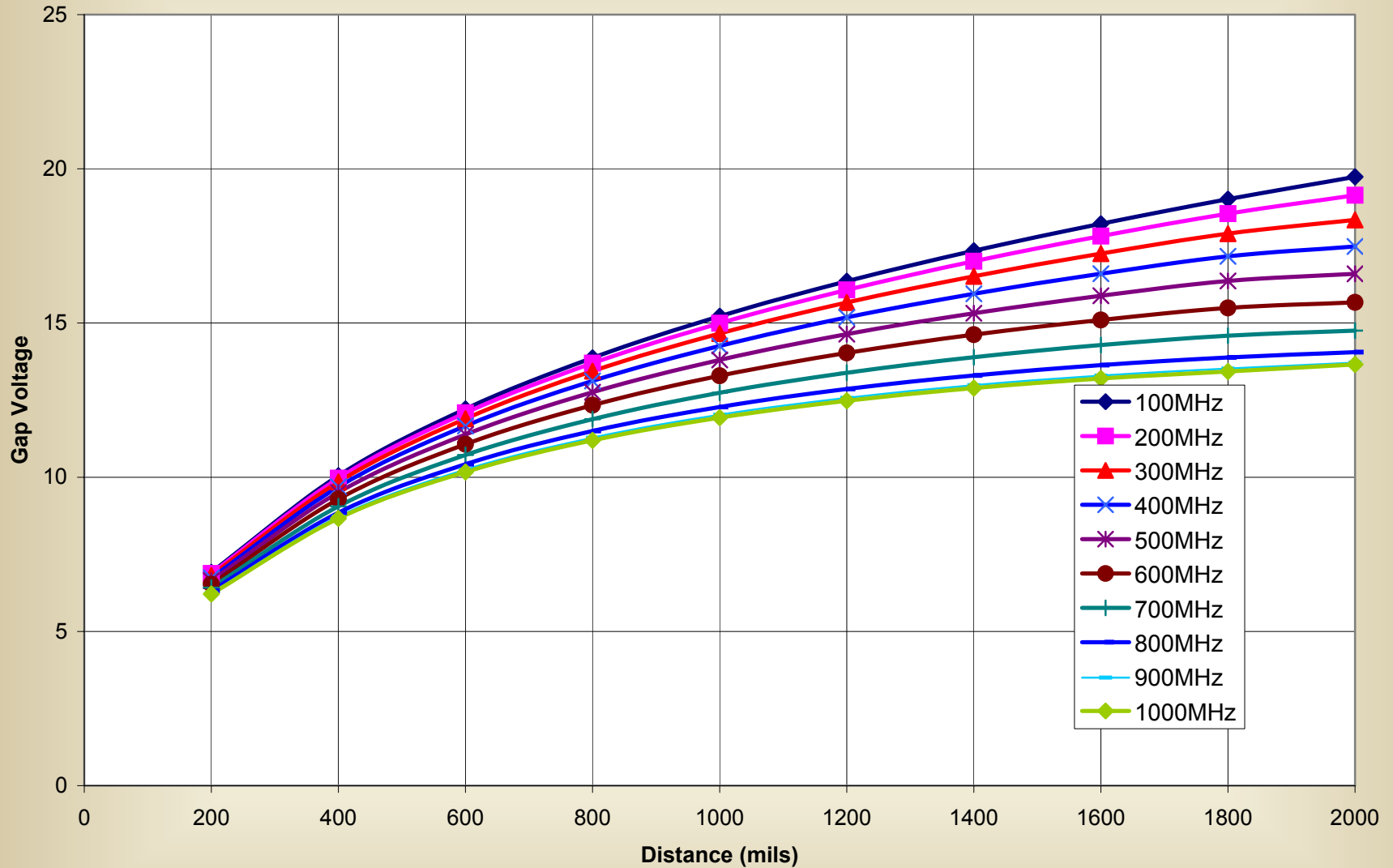


Stitching Caps with Via Inductance

Comparison of Maximum Radiated E-Field for Microstrip
With and without Split Ground Reference Plane and Stching Capacitors



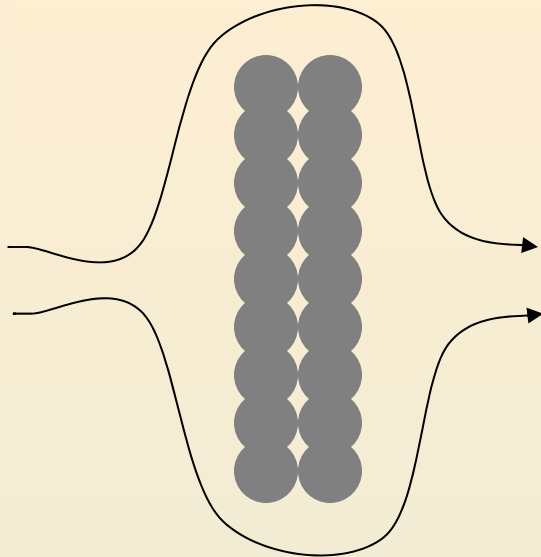
Example of Common-Mode Noise Voltage Across Split Plane Vs. Stitching Capacitor Distance to Crossing Point



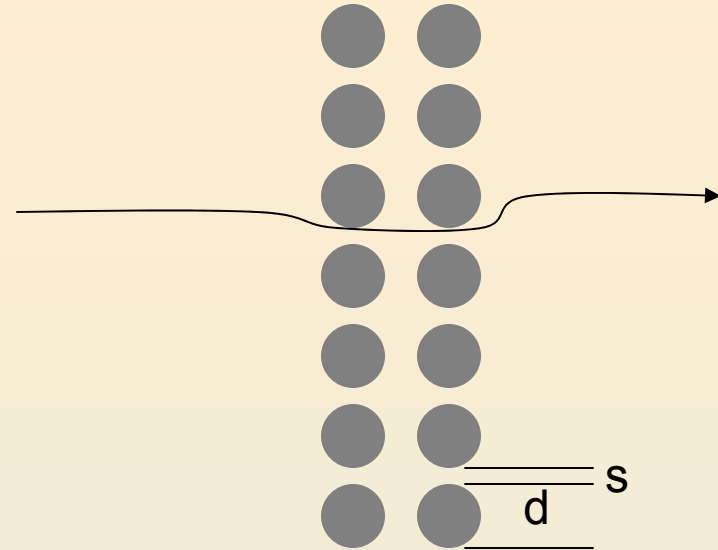
Are Stitching Capacitors Effective ???

- YES, at low frequencies
- No, at high frequencies
- Need to limit the high frequency current spectrum
- Need to avoid split crossings with ALL critical signals

Pin Field Via Keepouts??



Return Current must go around entire keep out area --- just as bad as a slot

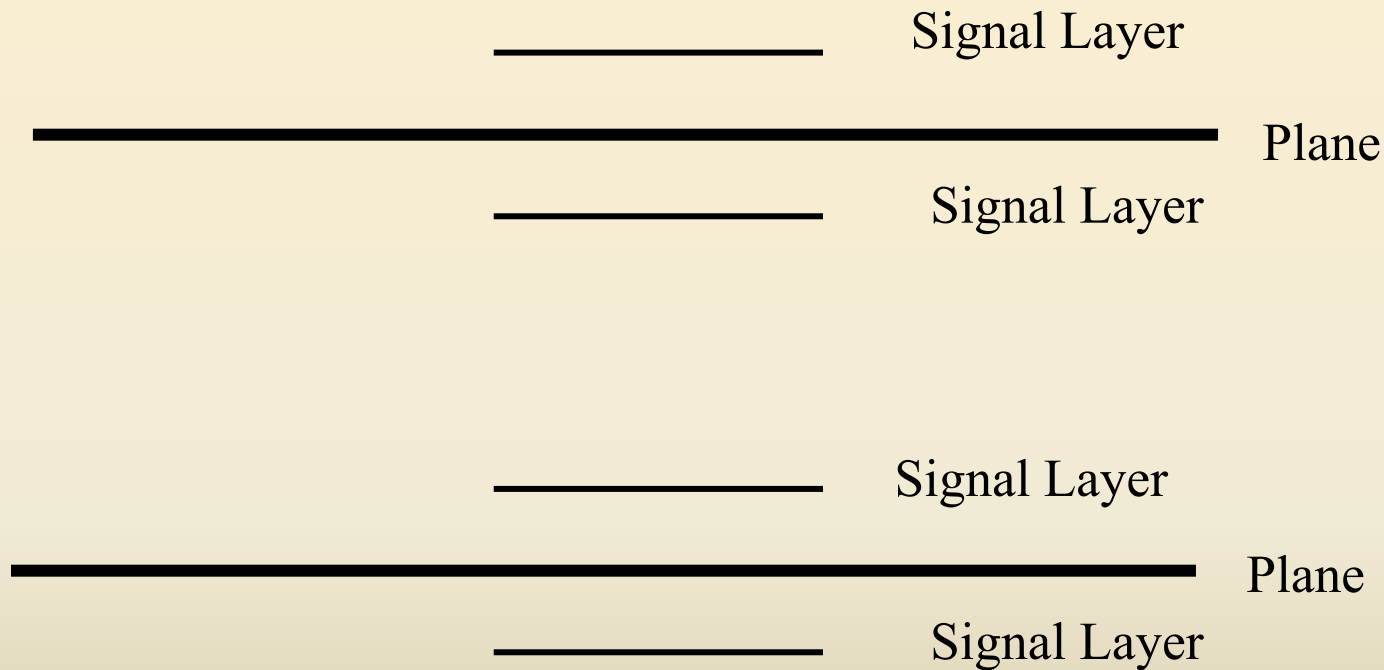


Return current path deviation minimal

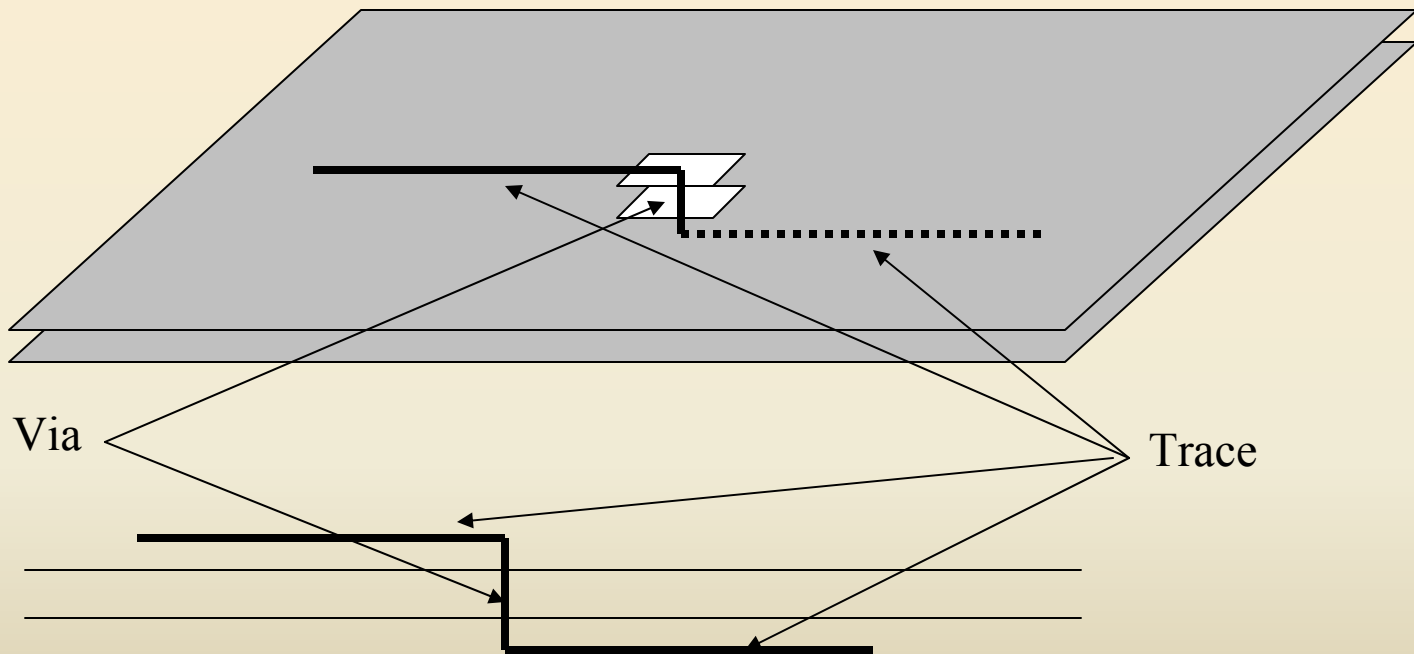
Recommend $s/d > 1/3$

Changing Reference Planes

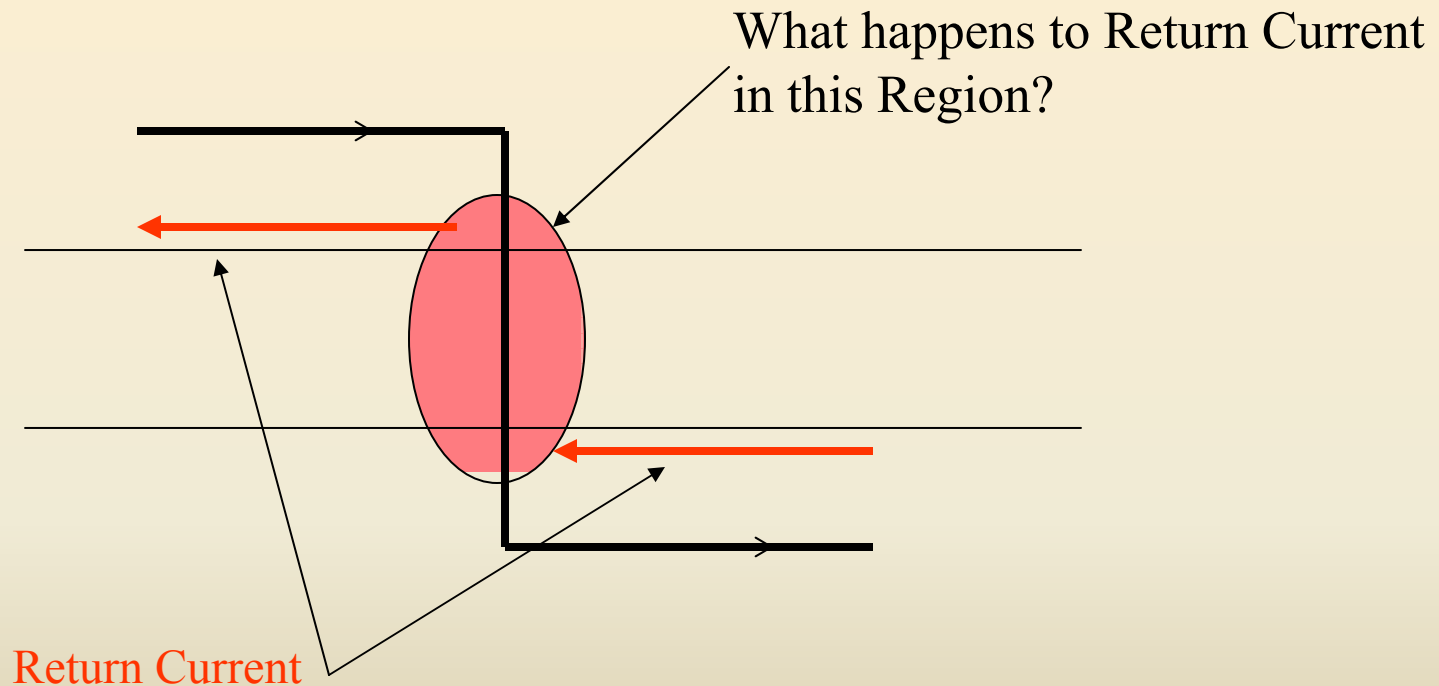
Six-Layer PCB Stackup Example



Microstrip/Stripline through via (change reference planes)



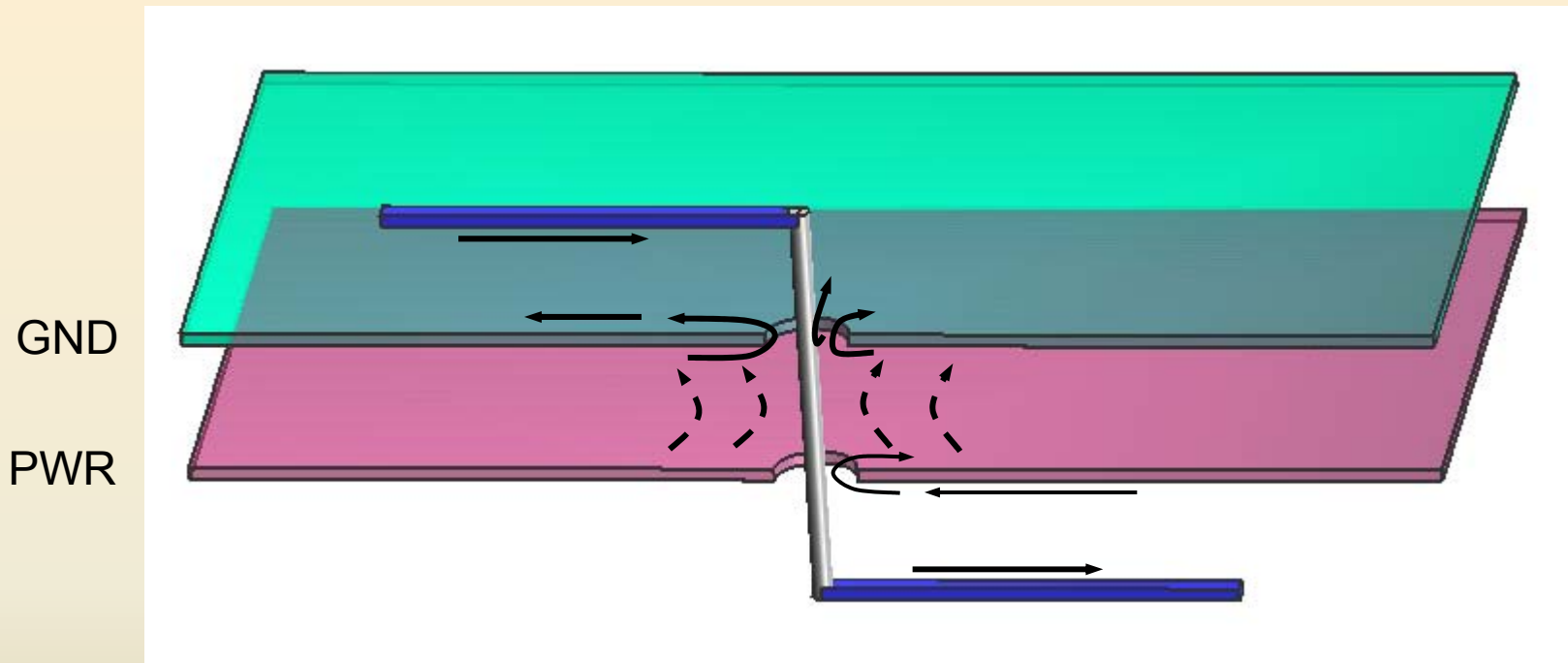
How can the Return Current Flow When Signal Line Goes Through Via??



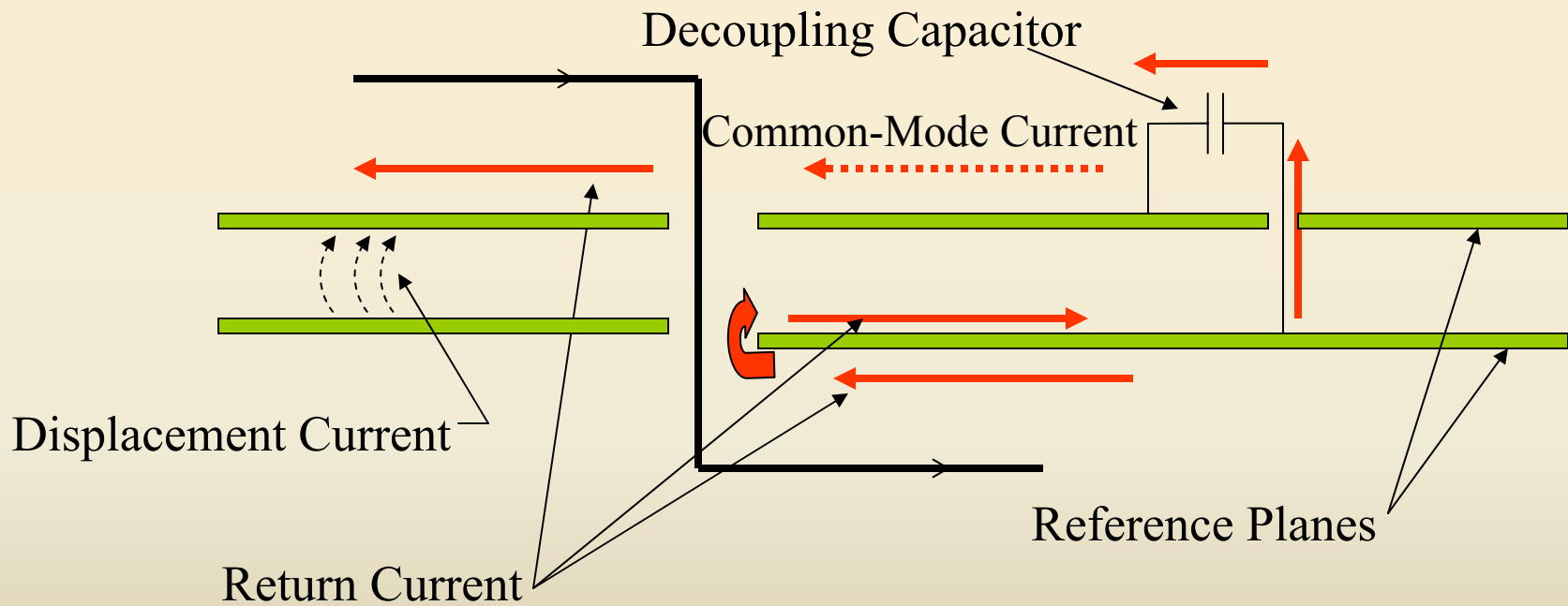
How can the Return Current Flow When Signal Line Goes Through Via??

- Current can NOT go from one side of the plane to the other through the plane
 - skin depth
- Current must go around plane at via hole, through decoupling capacitor, around second plane at the second via hole!
- Use displacement current between planes

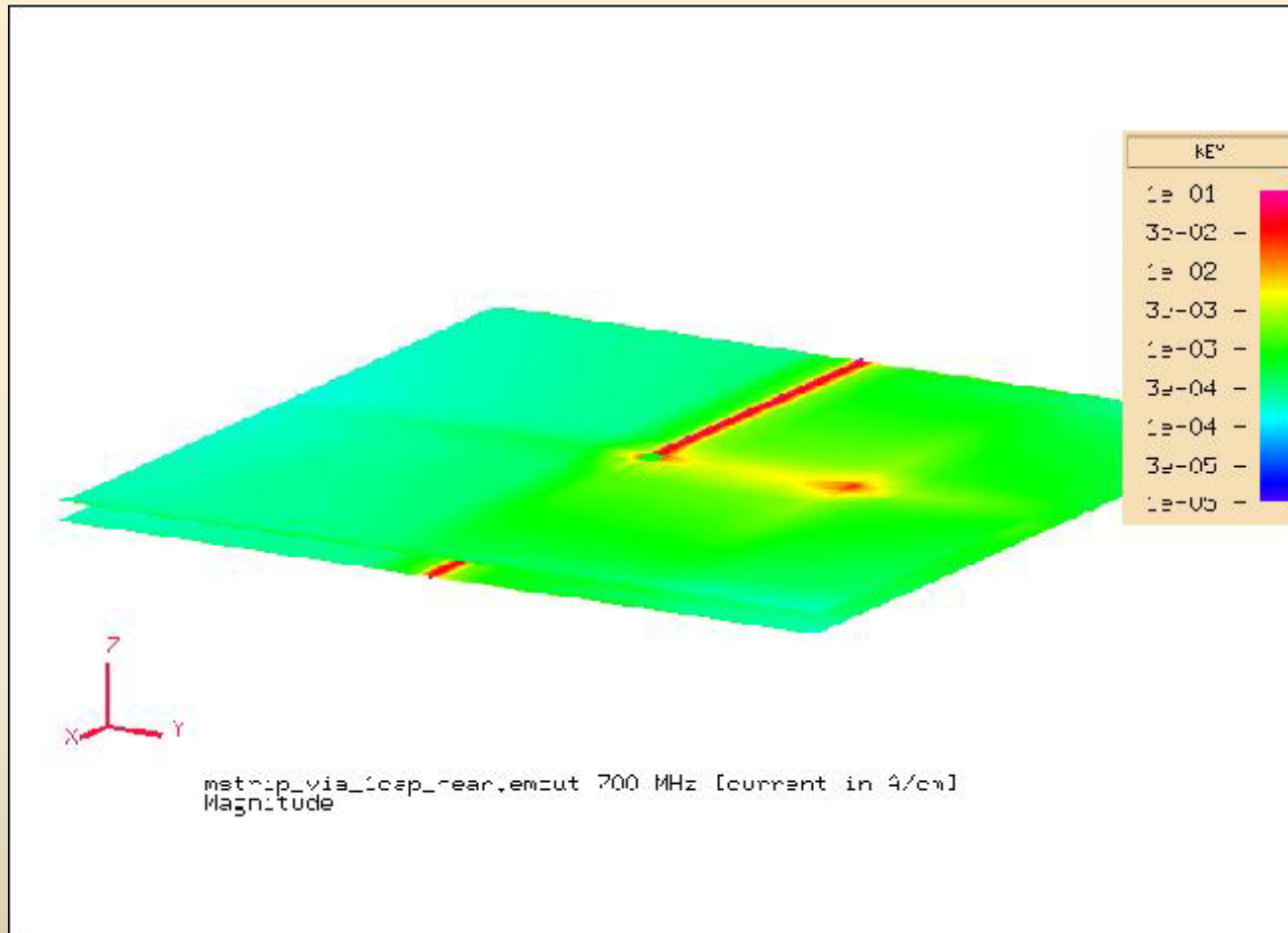
Return Current without Intentional Path



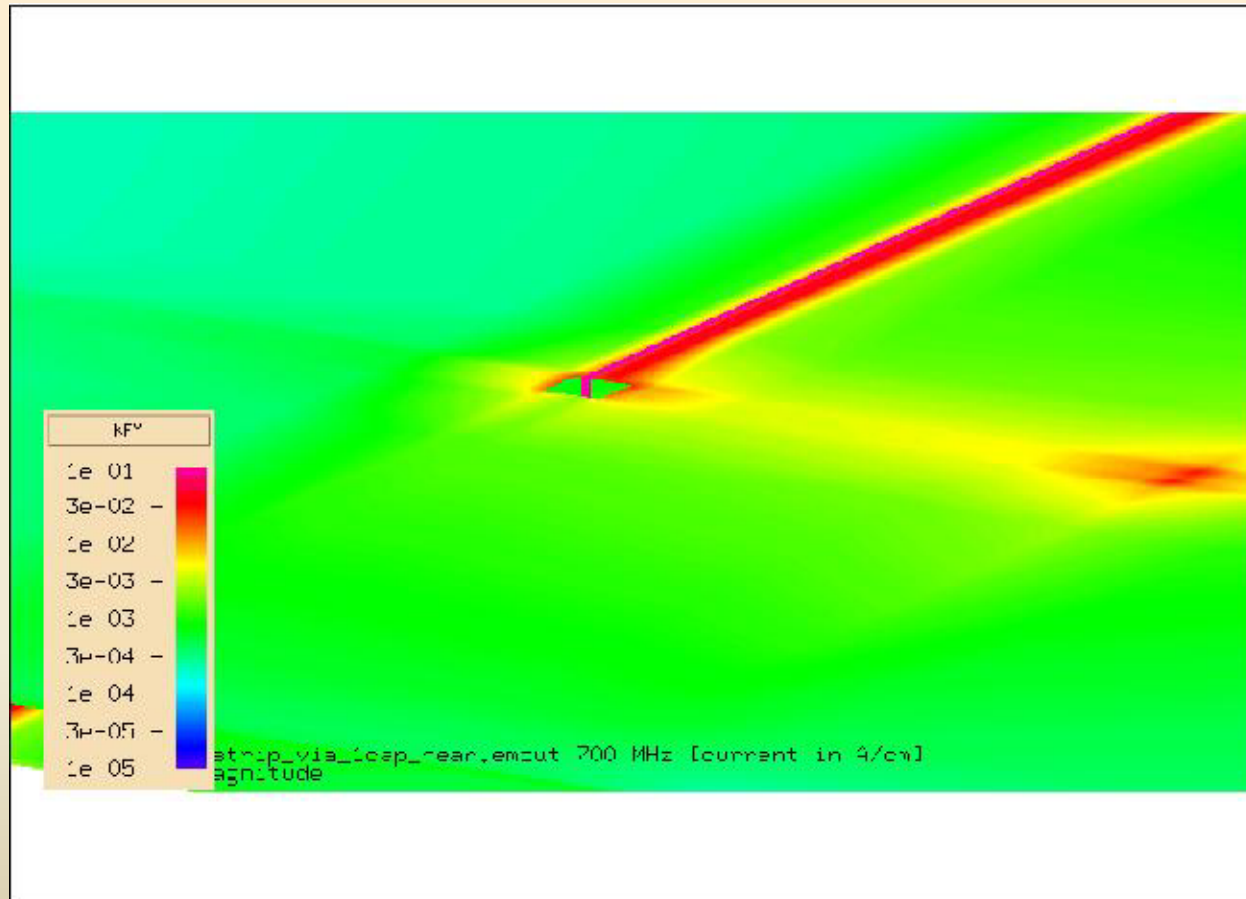
Return Current Across Reference Plane Change With Decoupling Capacitor (on Top)



RF Current @ 700 MHz with One Capacitor 0.5" from Via



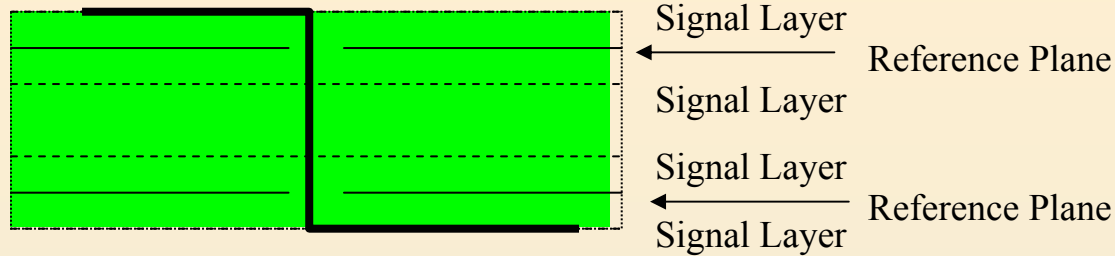
RF Current @ 700 MHz with One Capacitor 0.5" from Via (expanded view)



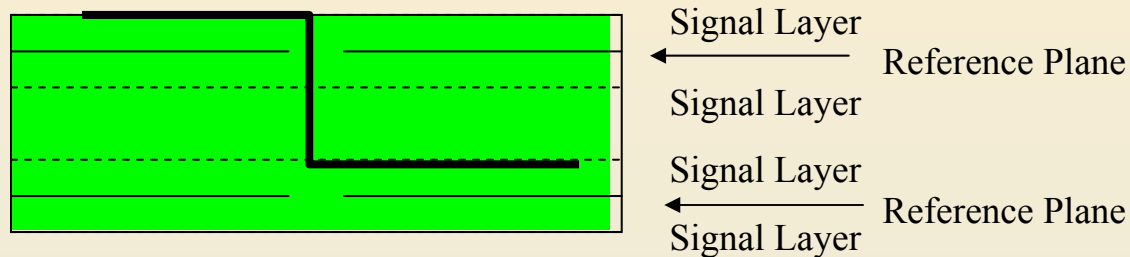
Possible Routing Options

Six-Layer Board

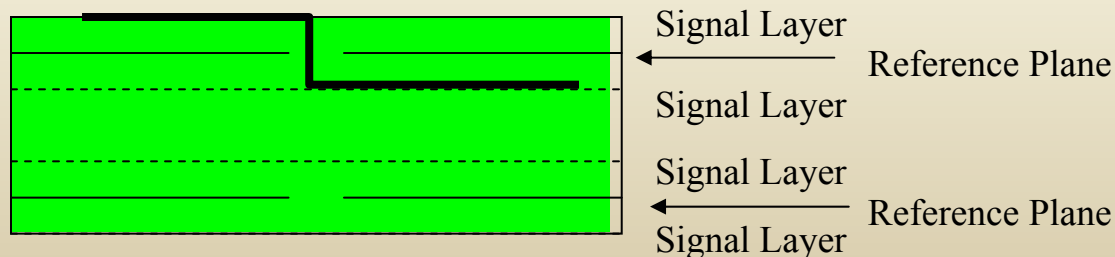
Bad



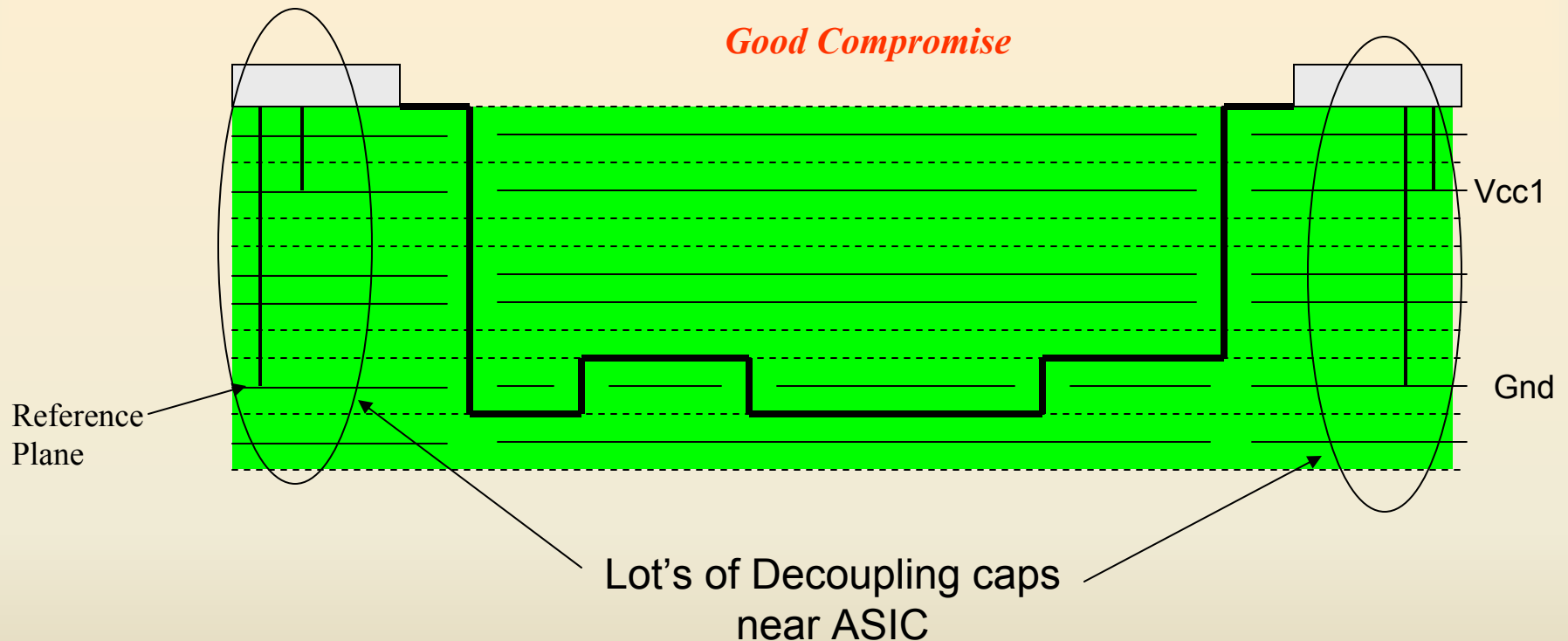
Bad



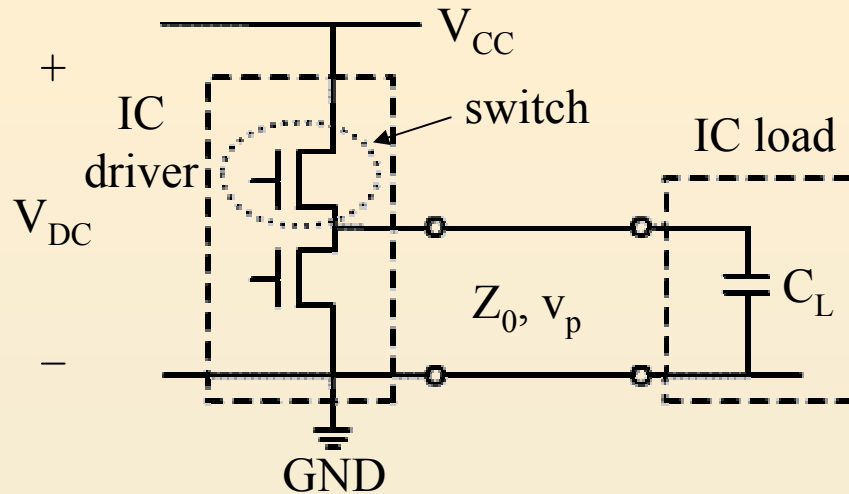
Good



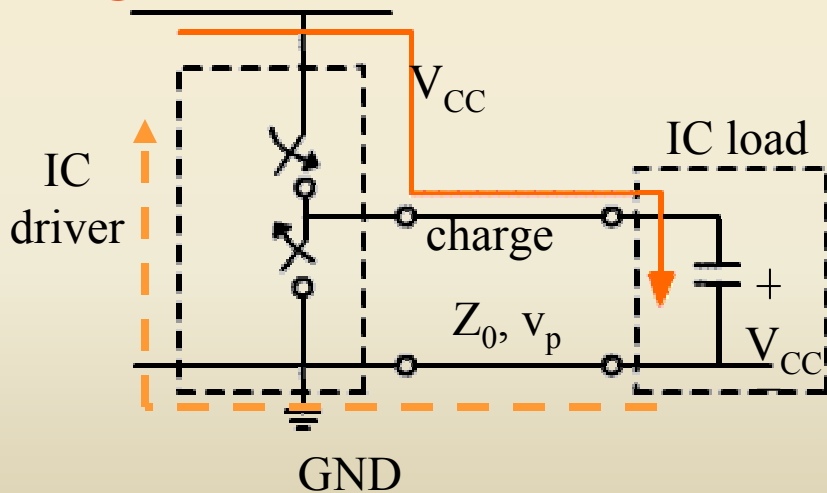
Compromise Routing Option for Many Layer Boards



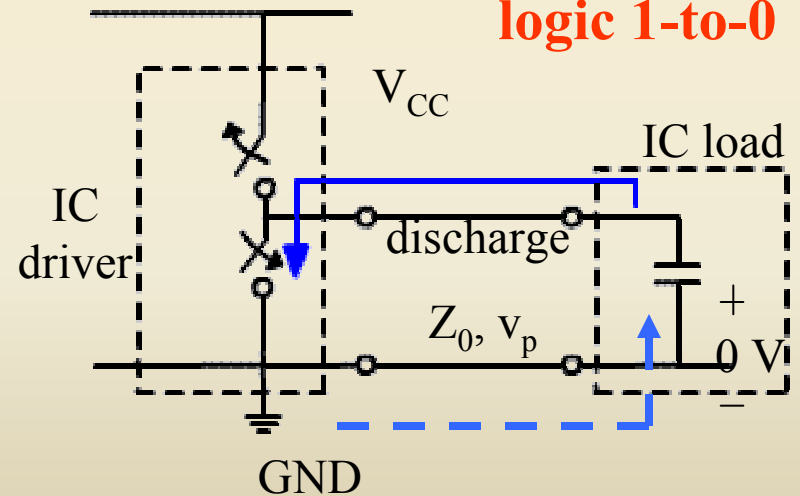
Typical Driver/Receiver Currents



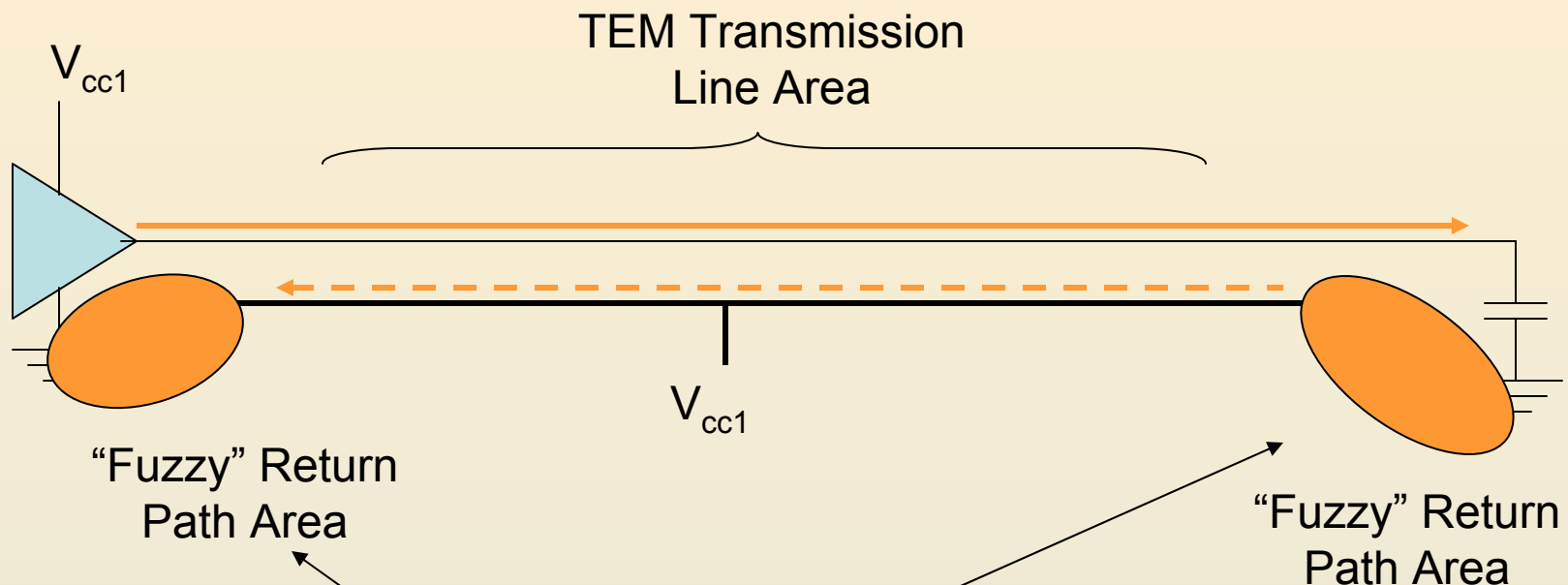
logic 0-to-1



logic 1-to-0



Suppose The Trace is Routed Next to Power (not Gnd)



"Fuzzy" Return Path Area

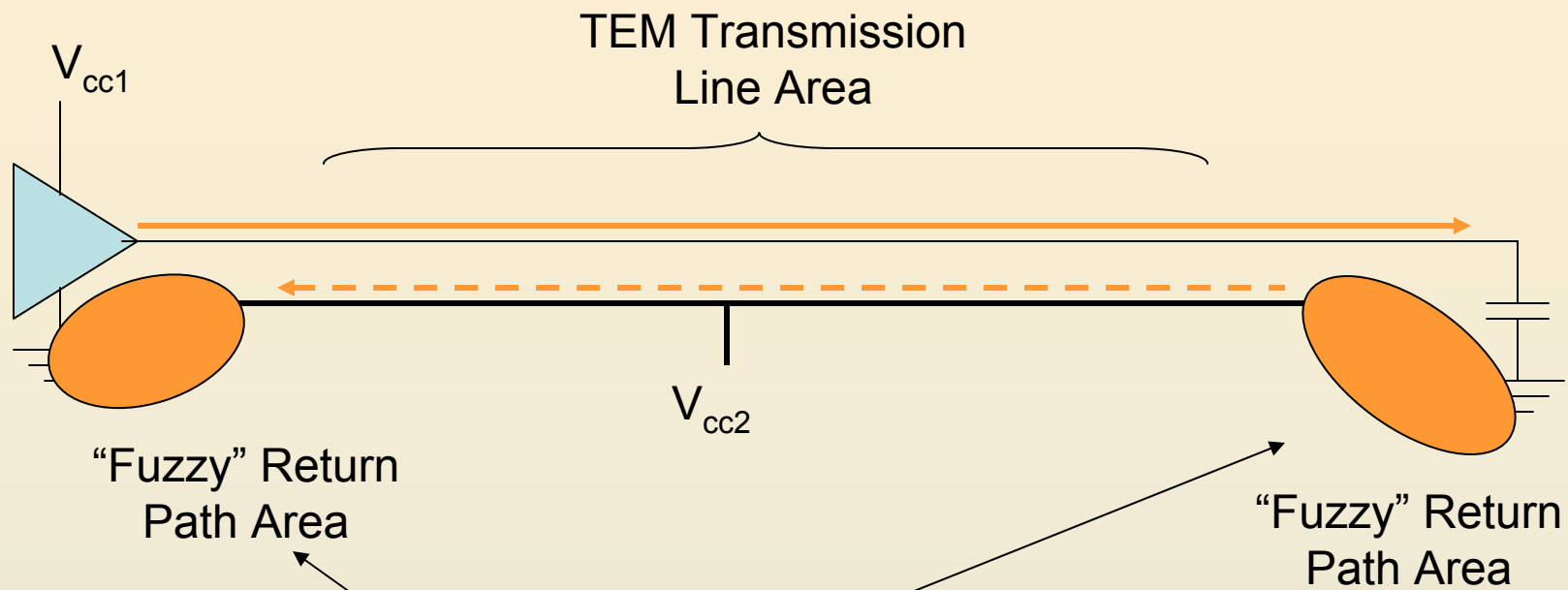
"Fuzzy" Return Path Area

Return Path Options:

-- Decoupling Capacitors

-- Distributed Displacement Current

Suppose The Trace is Routed Next to a DIFFERENT Power (not Gnd)



Return Path Options:

-- Decoupling Capacitors ??? May not be any nearby!!

-- Distributed Displacement Current – Increased current spread!!!

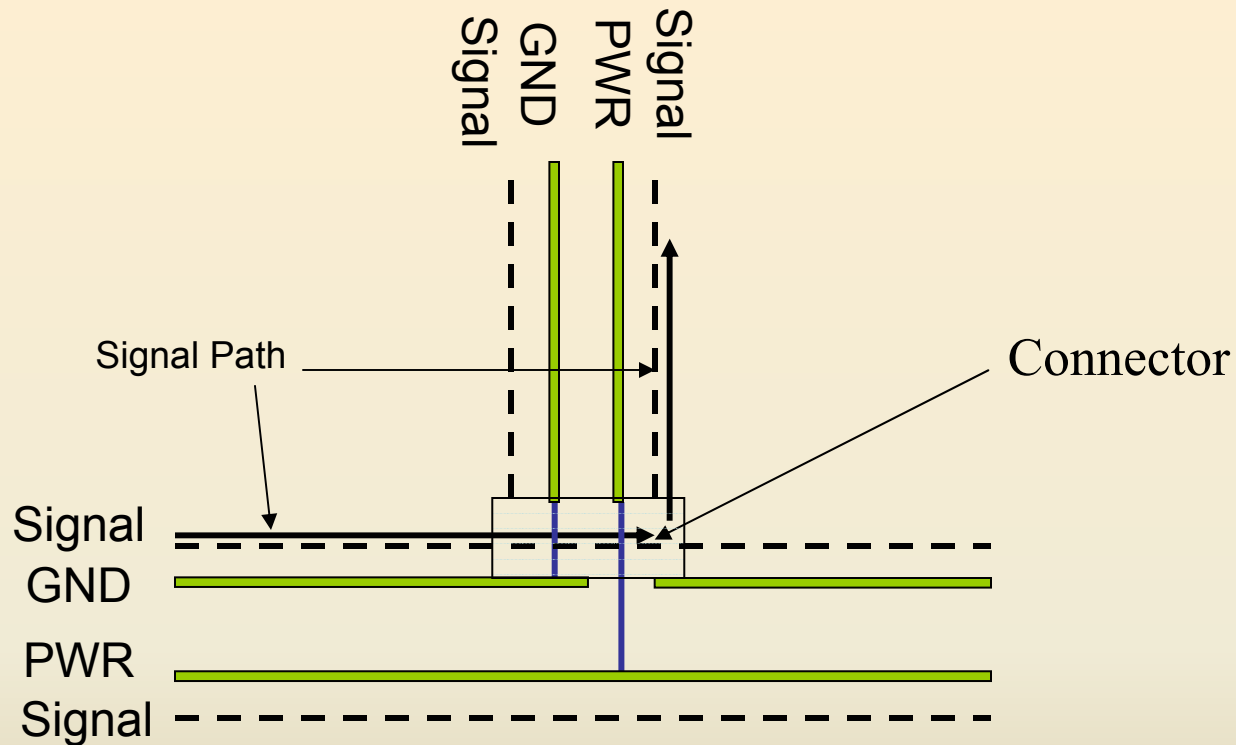
Via Summary

- ✓ Route critical signals on either side of ONE reference plane
- ✓ Drop critical signal net to selected layer close to driver/receiver
 - ✓ Many decoupling capacitors to help return currents
- ✓ Do **NOT** change reference planes on critical nets unless **ABSOLUTELY NECESSARY!!**
- ✓ Make sure at least 2 decoupling capacitors within 0.2" of via with critical signals

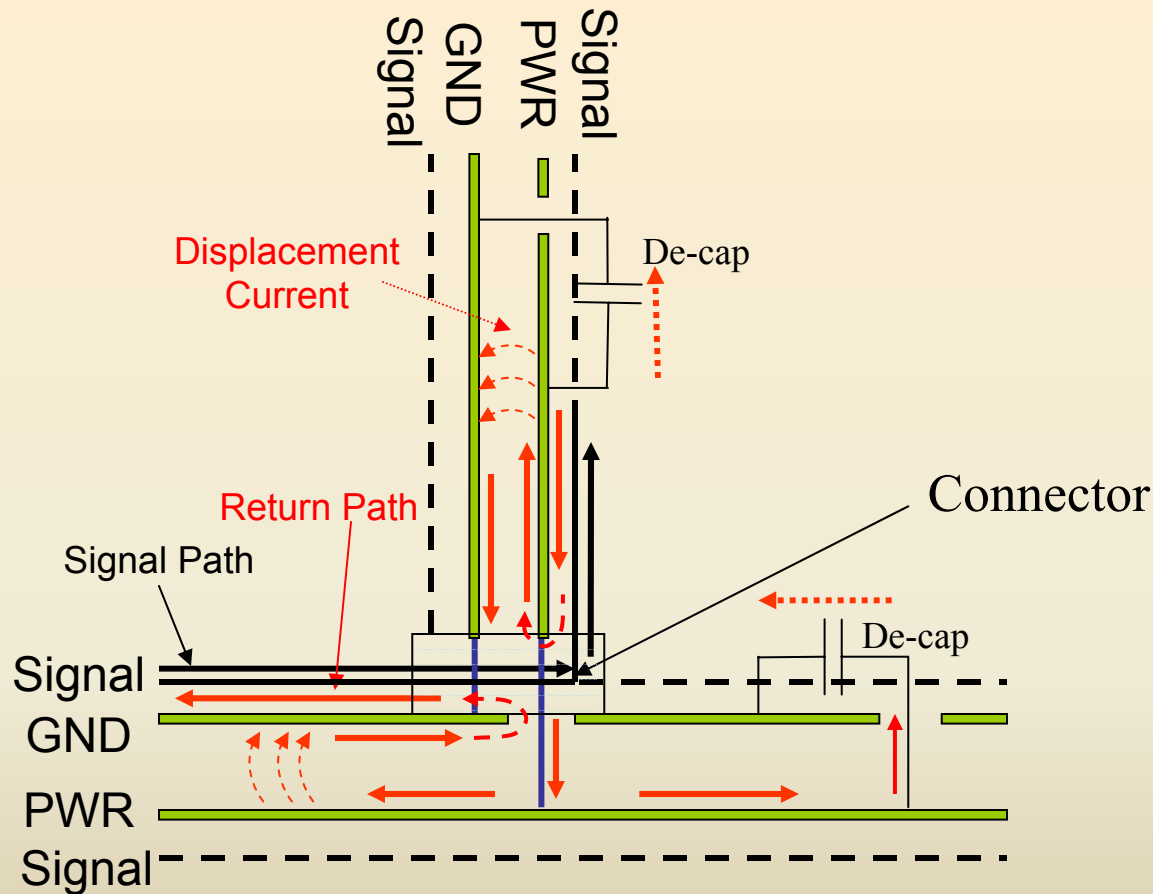
Mother/Daughter Board Connector Crossing

- Critical Signals must be referenced to same plane on both sides of the connector

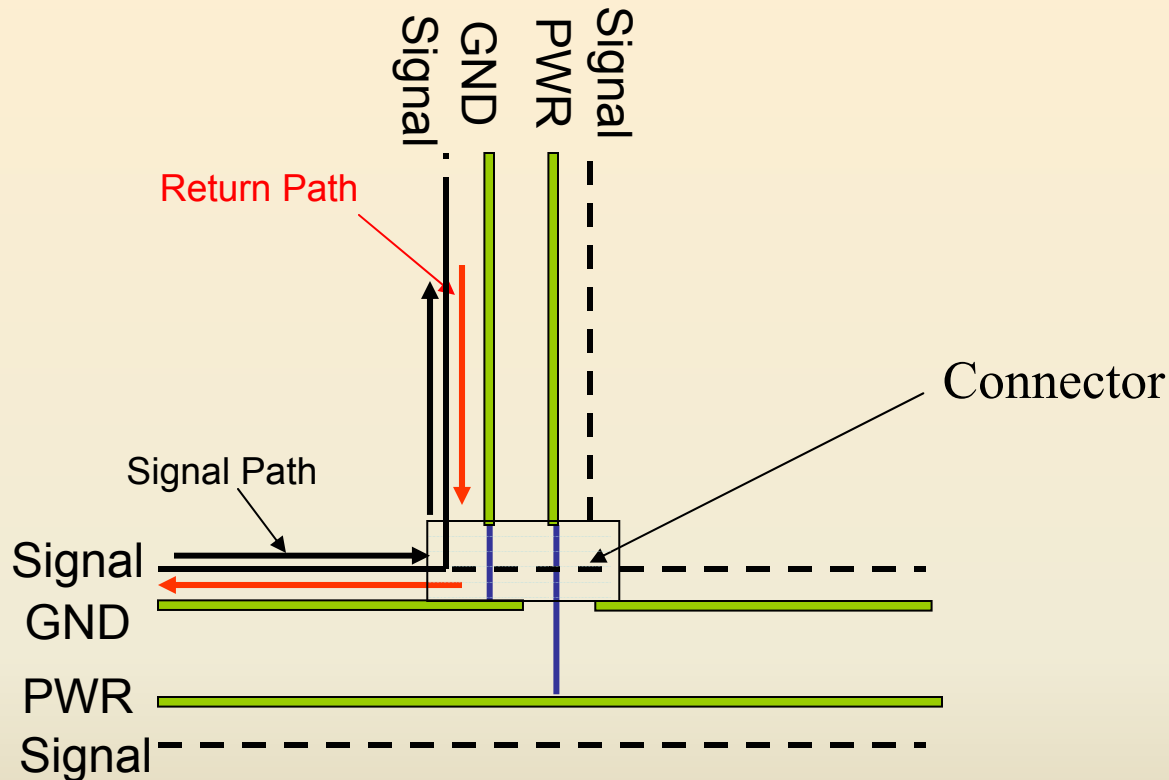
Mother/Daughter Board Connector Crossing



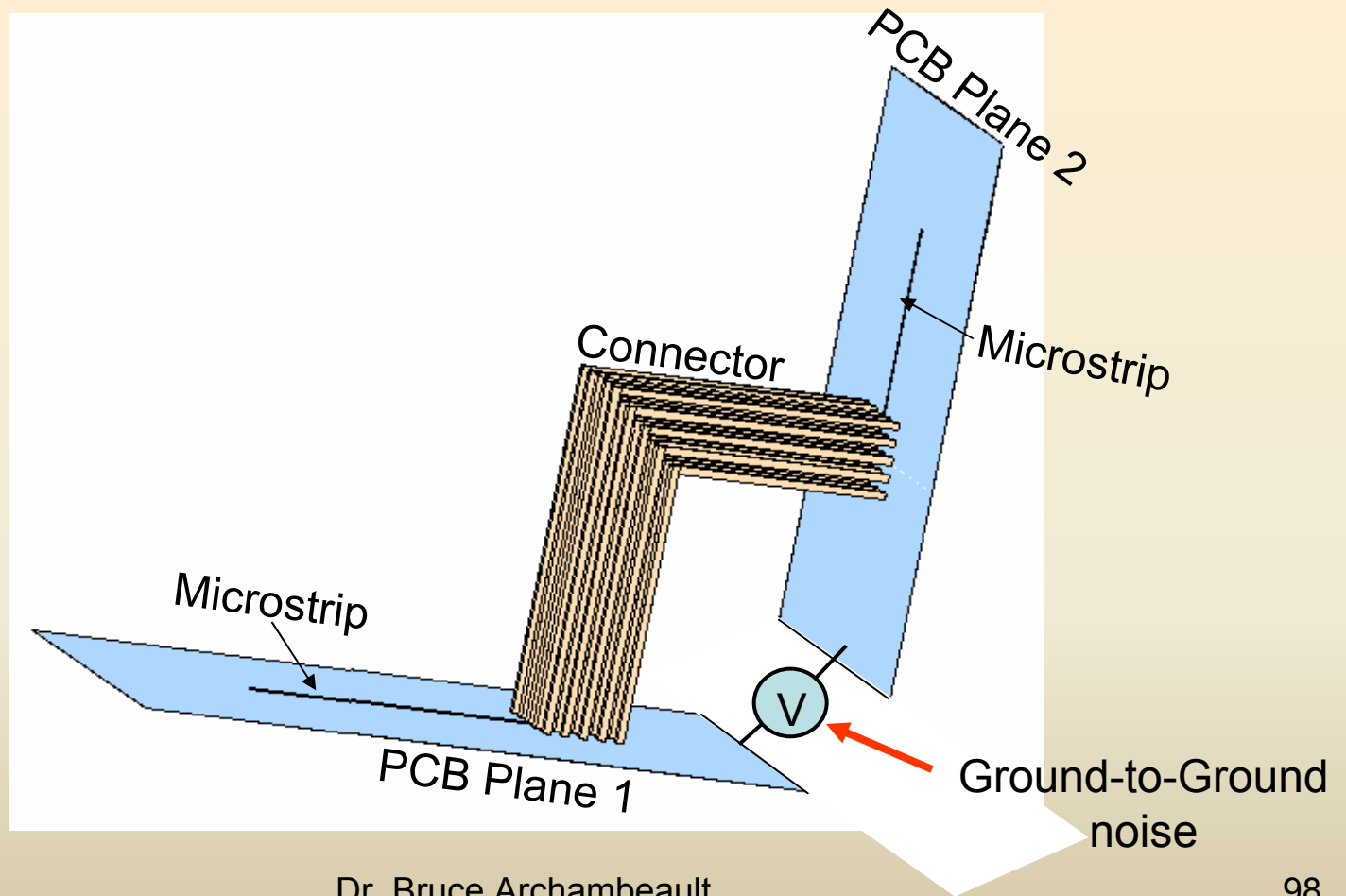
Return Current from Improper Referencing Across Connector



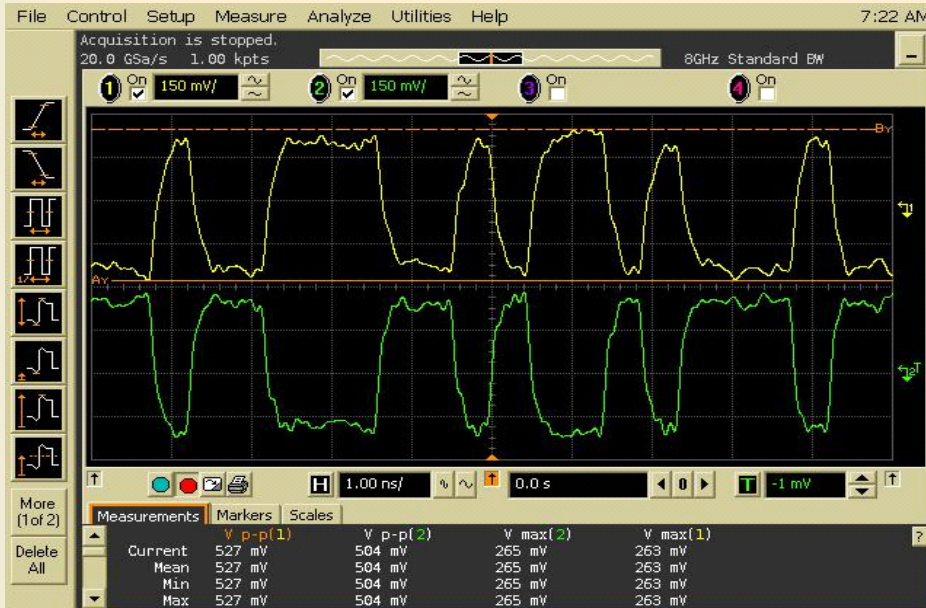
Return Current from Proper Referencing Across Connector



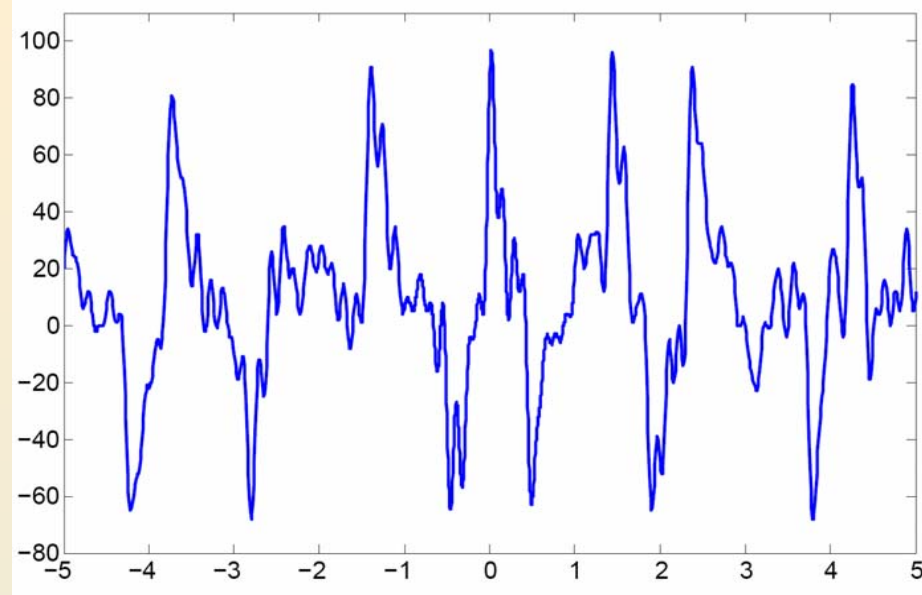
Board-to-Board Differential Pair Issues



Example Measured Differential Individual Signal-to-GND



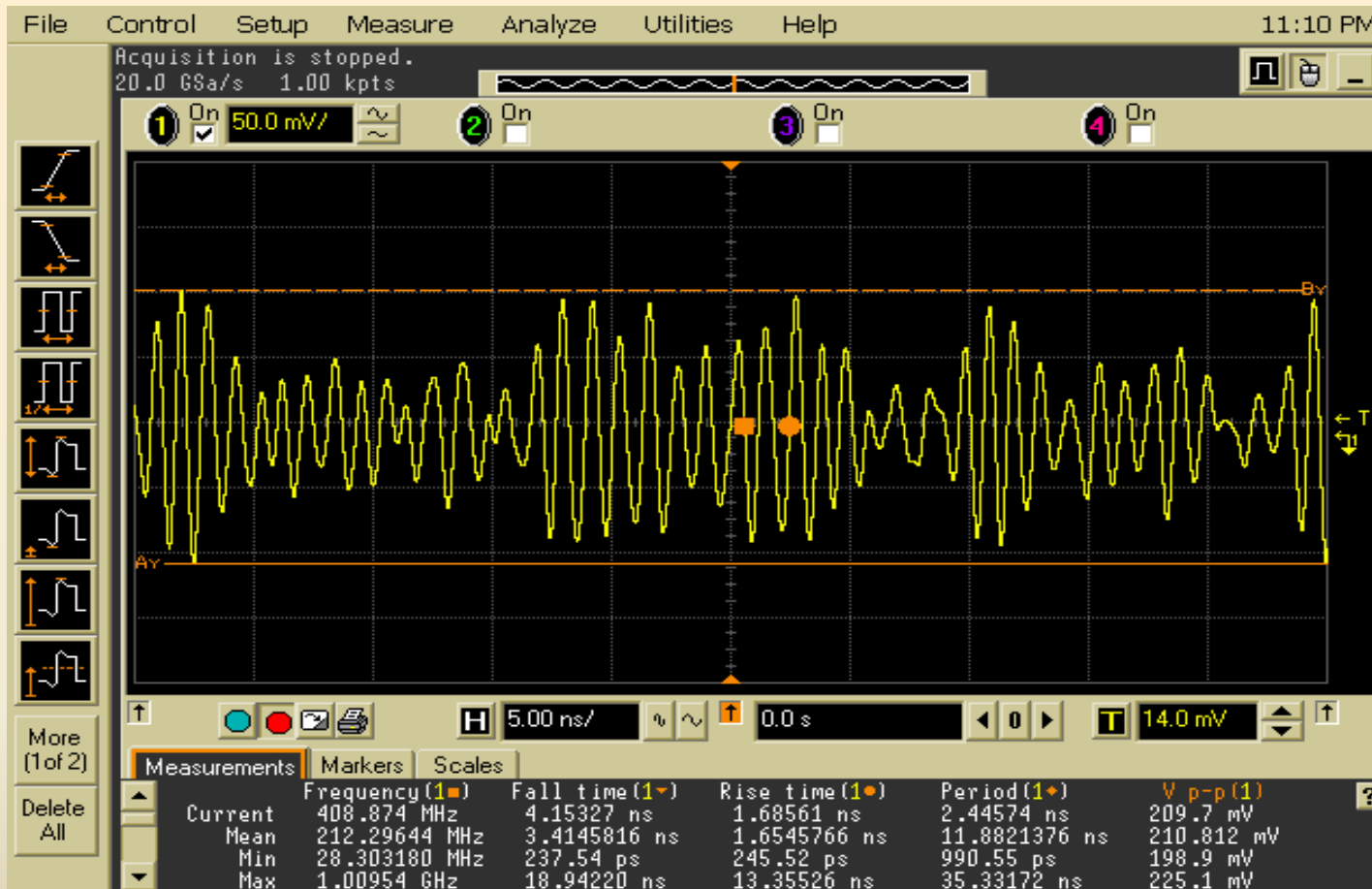
500 mV P-P (each)



Individual Differential
Signals ADDED

Common Mode Noise
170 mV P-P

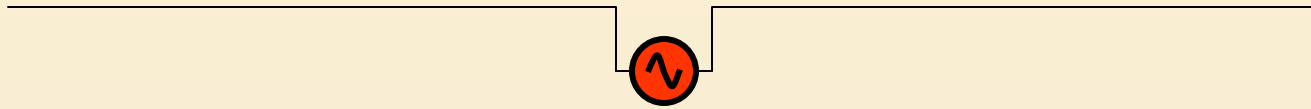
Measured GND-to-GND Voltage



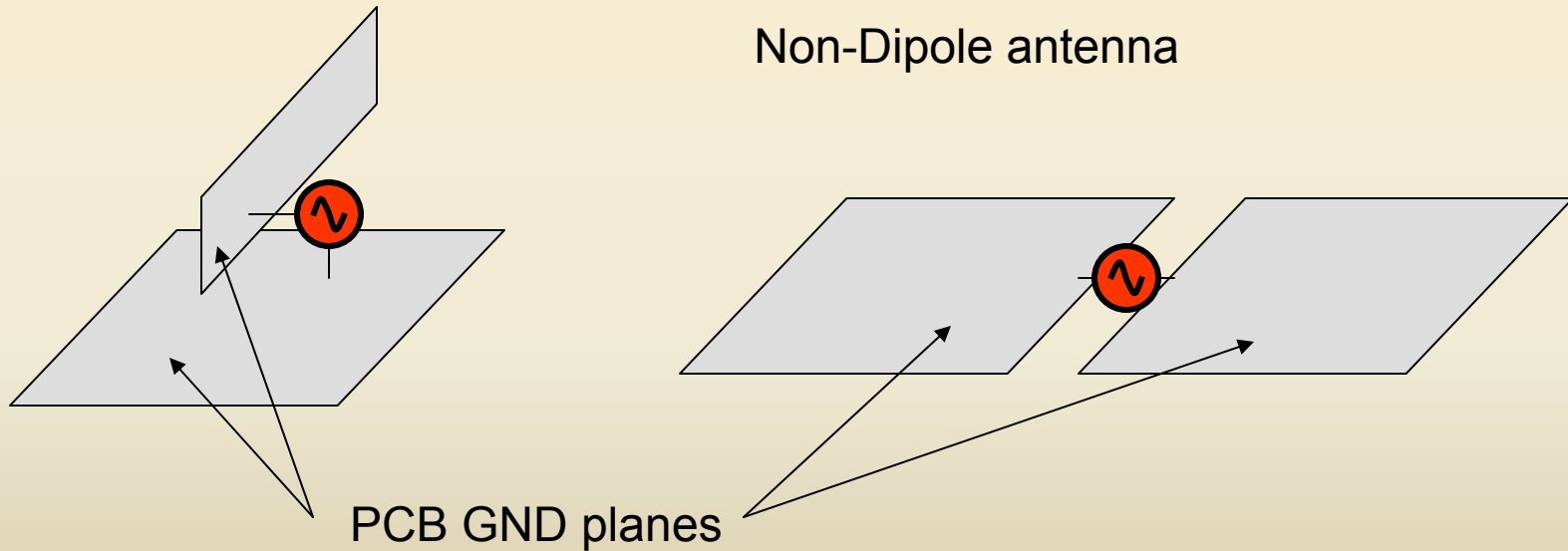
205 mV P-P

Antenna Structures

Dipole antenna

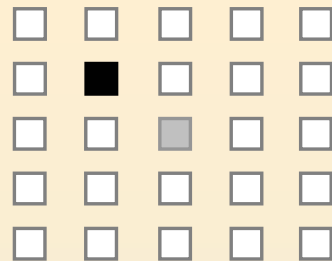


Non-Dipole antenna



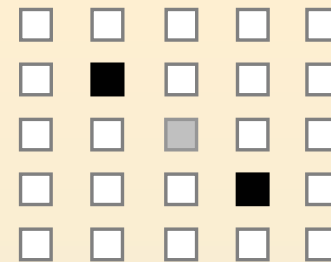
Pin Assignment Controls

Inductance for CM signals



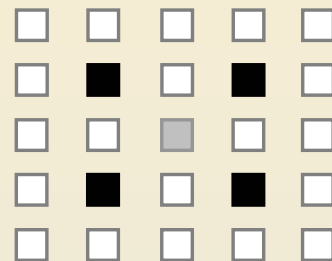
37.17 nH

(a)



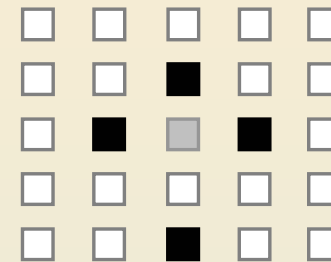
25.21 nH

(b)



16.85 nH

(c)



20.97 nH

(d)

■ Signal Pin

■ Related Ground Pins

How Many “Ground” Pins Across Connector ???

- Nothing **MAGICAL** about “ground”
- Return current flow!
- Choose the number of power and “ground” pins based on the number of signal lines referenced to power or “ground” planes
- Insure signals are referenced against same planes on either side of connector

Ground Myth Summary

- **THERE IS NO SUCH THING AS “GROUND”**
- Define which *reference* type is needed
- Plan the return current path
 - Avoid split reference planes & changing reference planes
- Differential signals have significant common mode, and must follow normal EMC rules



IEEE

