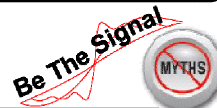
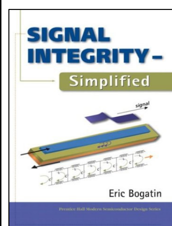


Ten Habits of Highly Successful Board Designers

or

Design for Speed:
A Designer's Survival Guide to Signal Integrity

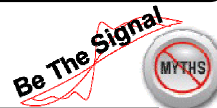


with
Dr. Eric Bogatin, Signal Integrity Evangelist,
Bogatin Enterprises, www.beTheSignal.com
eric@beTheSignal.com

Copies are available for download at www.beTheSignal.com

March 2009

Overview



- Interconnects are not transparent
- The design flow
- The six SI problems
- The 10 habits of highly successful designers

Interconnects are NOT Transparent

driver — 3 inch long PCB Trace — receiver

Vertical: 1 V/div offset: -2.0V
Horizontal: 5 ns/div delay: 0.000nsec

Signal Integrity Engineering is about how the electrical properties of the interconnects screw up the beautiful, pristine signals from the chips, and what to do about it.

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Hope Can't be Part of the Design Strategy in High-Speed Products

As speed goes up, your luck goes down

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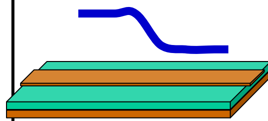
General Design Methodology

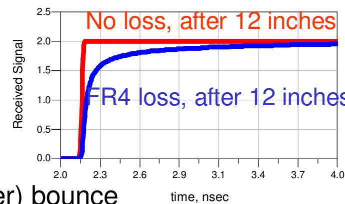
- Over riding product design goals
  - ✓ Meet specs: BER, power, freq, functionality, → define performance
  - ✓ Meet schedules → efficient design process
  - ✓ At lowest cost → (don't pay for extra design margin)
- Two categories of products
  - ✓ Performance driven
  - ✓ Cost-performance
- Methodology;
  - ✓ Identify the SI problems
  - ✓ Find the root cause
  - ✓ Establish design guidelines to minimize them

  } Understand the essential principles
  - ✓ "correct by design": use analysis tools to develop pre-layout design rules specific to your design
  - ✓ Use post layout verification tools to efficiently spin virtual prototypes

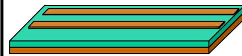
Why Interconnect are Not Transparent: The Most Important Signal Integrity Problems



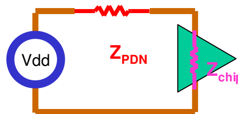
1. Reflection noise



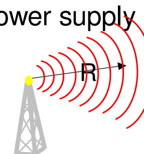
2. Cross talk



3. Ground (and power) bounce
4. Losses (@ Gbps)

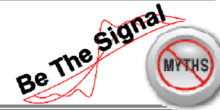


5. Rail collapse, voltage droop, power supply noise



6. EMI

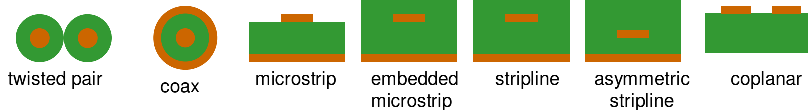
The Ten Habits of Highly Successful Designers



1. Design all interconnects as controlled impedance
2. Space out signals as far as possible
3. Don't cross the return current streams
4. Do not allow signals to cross gaps in return planes
5. Use return vias adjacent to EVERY signal via
6. Keep via stubs short
7. Use loosely coupled differential pairs, with symmetrical lines
8. Use multiple power and ground planes on adjacent layers with thin dielectric between them
9. Use shortest surface traces possible for decoupling capacitors
10. Use SPICE to simulate the impedance profile of the decoupling capacitors. Start with 1 uF, 100 nF, 10 nF and 1 nF, located in proximity to device.

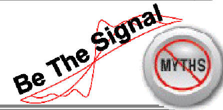
Habit #1: Design All Interconnects As Controlled Impedance

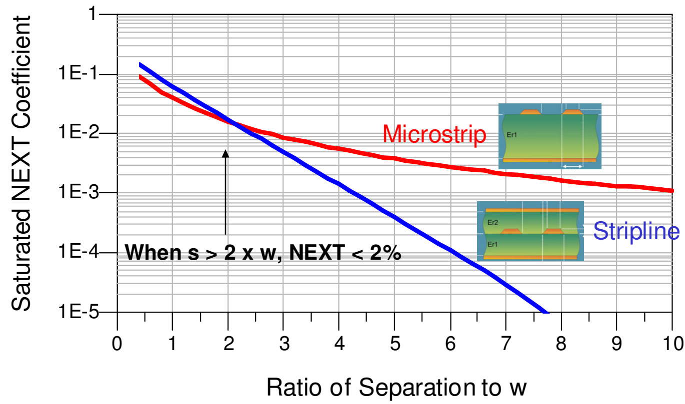
Controlled impedance structures



- Use uniform transmission lines to a target value ~ 50 Ohms
- Keep the instantaneous impedance the signal sees, constant
- Manage reflections at ends with termination scheme
- Use a linear topology, avoid branches, stubs

Habit #2: Space Out Signals As Far As Possible

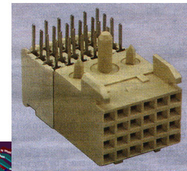


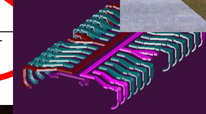


For worst case NEXT
in a bus, keep NEXT < 2%
Design separation > 2 x w, MS or SL

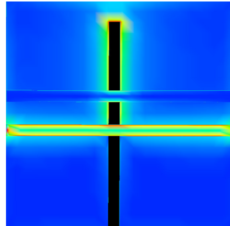
Habit #3: Don't Cross The Return Current Streams

- Re-calibrate your intuition about ground
  - ✓Return path for signals
  - ✓Return path for power
- Never forget: If current flows in "ground", there will be a voltage drop due to
  - ✓I x R
  - ✓L x dI/dt
- Ground bounce: cross talk between signal lines with overlapping return currents
  - ✓Most important design guideline: **"Don't cross the streams!"**
  - ✓Avoid overlap of return currents

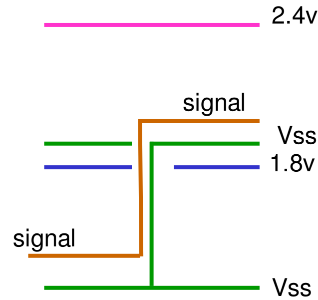




Habit #4: Do Not Allow Signals To Cross Gaps In Return Planes



Don't route signals between split planes
But if you do…
- route signal layer close to continuous Vss
- far from split plane layer



- Problems:
  - ✓ Reflection noise
  - ✓ Ground bounce
  - ✓ EMI

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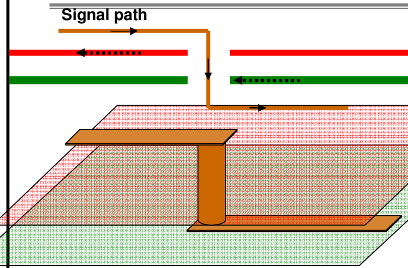
Ground Bounce Between Two Return Planes



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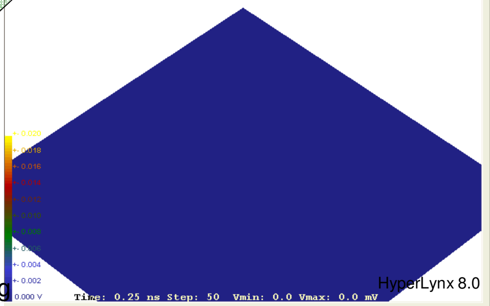
20 mV voltage between the planes, full scale

10" x 10"
h = 30 mils
RT = 0.2 nsec
I = 20 mA



Features of ground bounce:
1. Long range
2. Can be large
3. Additive with more vias switching
4. Return current injects noise into the planes' cavity

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How to Minimize the Switching Noise?

"a lot is good, more is better and too many is just right"
- Frank Schonig

Add an adjacent return via

Add 4 adjacent return vias

HyperLynx 8.0

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Ideal Return Via Configuration to Minimize Ground Bounce

Minimizes the spreading of the return currents from each via

Ideal:

A Good Habit:

Reduces the spreading of the return currents from each via

Worst case:

Will cause ground bounce, inject "long range" noise in the plane
Problem for very low noise boards

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A Stub Discontinuity

Be The Signal

Z0 bad
Len

Examples: test lines to relays, via stubs, a branch

	RTnsec	Len	Z0_bad
Value	0.5	0.5	50
Max	1	1	100
Min	0.02	0.05	5

V_stub, V
time, nsec
stub

Keep impedance of stubs high
Keep Len (inches) < RT (nsec)

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How to Avoid Via Stub Discontinuities?

Be The Signal

- Only use top layer to bottom layer vias- no stubs
- Restrict layer transitions from near top to near bottom
  - ✓ From top layer to near bottom layer
  - ✓ From near bottom layer to near top layer
- Use blind or buried vias
- Back drill long stubs
- Design stack up for thinner board
- For BR < 5 Gbps, try to keep via stubs < 60 mils long

back drilled

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Habit #7: Use Loosely Coupled Differential Pairs, With Symmetrical Lines

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Common Noise rejection
Higher Interconnect Density
Thinner Dielectric
Lower Conductor Loss
tight
Sweet spot s ~ 2w
loose

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Habit #8: Use Multiple Power And Ground Planes On Adjacent Layers With Thin Dielectric Between Them

Be The Signal MYTHS

A

h

$$C = \varepsilon_0 Dk \frac{A}{h}$$

$\varepsilon_0 = 0.225 pF/in$

Dk ~ 4

$$\frac{C}{A} = \frac{1}{h}$$

h in mils, C/A in nF/inch^2

h = 3 mils, C/A = 0.3 nF/in^2
In 10 sq inches, C_{planes} ~ 3 nF
On-chip capacitance ~ 300 nF

Thin dielectric provides low spreading inductance between decoupling capacitors and packages:
- Near the surfaces
- Multiple layers in parallel

TOP
Vdd
GND
InnerSignal1
InnerSignal2
GND
Vcc
BOTTOM

Habit #9: Use Shortest Surface Traces Possible For Decoupling Capacitors

1. Capacitor trace inductance
2. Via inductance to the planes
3. Spreading inductance in the planes
4. Package mounting inductance

For 3 mil thick dielectric to top plane: ~ 100 pH/sq
For 10 mil thick dielectric to top plane: ~ 320 pH/sq

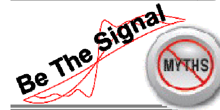
Common Rule of Thumb: Add 3 Capacitors per pin pair: 3 Different Values or 1 Value?

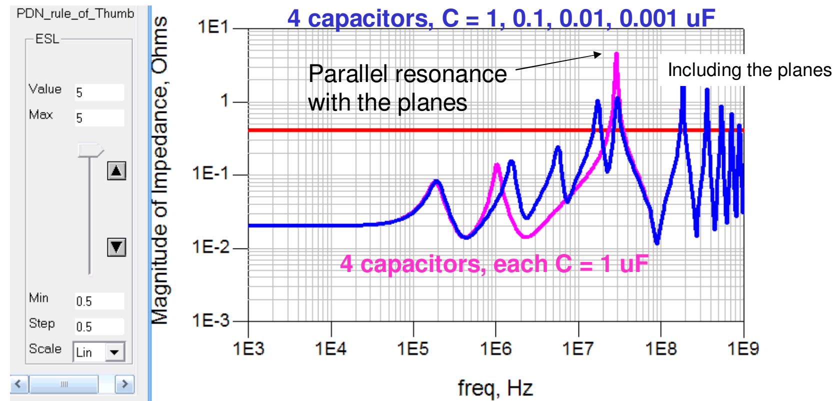
ESL = 5 nH

ESR = 0.04 → 0.3 Ohms

Not much difference between them

Habit #10:
Use SPICE to simulate the impedance profile of the decoupling capacitors. Start with 1 uF, 100 nF, 10 nF and 1 nF, located in proximity to device.





Reduce impact of plane parallel resonance by using multiple, small value capacitors, with as low an ESL as possible

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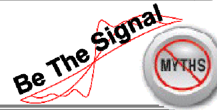
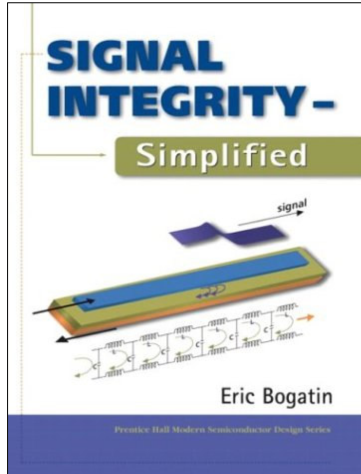
For More Information





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