IEEE COMPEL 2014 Schedule

	June 22, Sunday		June 23, Monday		June 24, Tuesday		June 25, Wednesday
				8:15	**Keynote Speech**		
		8:30	**Opening Session**				
		9:00 10:45	**Oral Session 1: Modeling & Simulation** Assembly Hall	9:00 10:45	**Oral Session 4: Circuit Modeling & Simulation** Assembly Hall	9:00 10:45	**Oral Session 7: Device & Component Modeling & Simulation** Assembly Hall
			Coffee Break Cafeteria		Coffee Break Cafeteria		Coffee Break Cafeteria
		11:15 13:00	**Oral Session 2: Digital Control** Assembly Hall	11:15 13:00	**Oral Session 5: Advanced Control of Converters** Assembly Hall	11:15 13:00	**Oral Session 8: Control Techniques** Assembly Hall
			Lunch Restaurant		Lunch Restaurant /Committee meeting		Lunch Restaurant
15:00 16:30	Advanced Control Techniques for Buck Type DC-DC Converters **Tutorial 1.** Room 23	14:30 16:10	**Oral Session 3: System Power Management** Assembly Hall	14:30 16:10	**Oral Session 6: PV Systems** Assembly Hall		Buses start at 15:00 Altamira Museum, Neocave (recreation of the Altamira cave), Santillana del Mar
	Coffee Break Cafeteria		Coffee Break Cafeteria		Coffee Break Cafeteria		
17:00 18:30	Extreme Efficiency Power Electronics **Tutorial 2.** Room 23	16:45 18:45	**Poster Session 1** Room E4	16:45 18:45	**Poster Session 2** Room E4		
				18:45 19:30	**IEEE PELS-IES Spanish Joint Chapter Meeting**		
		20:00	**City Hall Reception** City Hall			20:00 21:00	**Award Reception COMPEL 2015 Presentation** Torre de Don Borja
						21:00 23:00	**Banquet** Parador Nacional Santillana

Tutorial 1. Advanced Control Techniques for Buck Type DC-DC Converters**. Javier Uceda, Jesús Oliver and Pedro Alou.** Universidad Politécnica de Madrid

Tutorial 2. Extreme Efficiency Power Electronics. **Johann W. Kolar.** Swiss Federal Institute of Technology

Opening Session. UC Welcome **by Ángel Pazos Carro.** Vice-rector for Research Activities of the University of Cantabria

Keynote Speech. Understanding Current Loop Gain? **Dong Tan.** President of IEEE PELS