IEEE ComSoc
IEEE Communications Society
Bangalore Chapter

News@ComSoc Bangalore

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About IEEE ComSoc Chapter Bangalore Newsletter

The IEEE ComSoc Chapter Bangalore Newsletter let us call it ComSoc Bangalore India Newsletter (ComSoc-BIN) includes news useful to its members, nonmember and highlights most important technology development. It also highlights important concluded and upcoming events. Links for few important topics from current issue of *IEEE Communication Magazine are also embedded.*

Inside this issue:

Editor Message

Dear Reader,

Greetings from IEEE ComSoc Bangalore Chapter! It is a privilege to bring this newsletter to the communication engineering community of Bangalore Section and India.

As you are aware, the newsletters of an organization serve as the archives of the activities and have a major role to play in the history of the organization. We wish the ComSoc-BIN, apart from the record of activities of IEEE ComSoc Bangalore Chapter to include some articles of current interest. The prime aim of this newsletter is to provide a way to communicate with the members and the community at large in regular intervals. Usually, we get a very few occasions to communicate with our valued colleagues. Such occasions normally come during the IEEE AGM, conferences, workshops and other gatherings such as invited talks. We feel we need to communicate with you more frequently. Besides that, we think that each member is important and should get a direct communication from ComSoc.

We hope this newsletter will serve our purpose and certainly help us communicating better.

At this moment, we plan to bring quarterly (3 issues in a year) newsletters which we fondly call Communication Society Bangalore India Newsletter (ComSoc-BIN). The approximate length of ComSoc-BIN will be around 10 pages depending on the articles and items we get for each issue.

I would like to thank all authors who have submitted the topic of interest and current technology. There have been more submission but some of them could not be accommodated mainly because of scope and relevance. Finally, I request the members of the community to come forward with their contributions, suggestions and feedback. It will help us serve you better. Please use the email of ComSoc chair for these communications. Let us have a new beginning!

With best regards,

Sudhir K. Routray, PhD

Chairman Message

Dear IEEE Members,

At the outset, I express my sincere thanks to all the IEEE ComSoc members in Bangalore for giving me the opportunity to serve as the Chair in 2017. It is a great opportunity, but at the same time is a big responsibility. I would like to rise up to the expectations of the members to the best of my ability.

I also express my happiness to have a very strong, energetic and motivated team including office bearers and ExCom members to take forward the activities of ComSoc in this year. Each of them is committed to the cause of IEEE and is ready to put on their best. My hearty thanks and appreciation to all of them for shouldering such responsibilities.

The Newsletter, ComSoc-BIN (Communication Society Bangalore India Newsletter) is the latest initiative by the chapter. I strongly believe, the ComSoc-BIN will mature with each edition and will get a wide popularity.

I congratulate and thank all the contributors and companies who extended their support in bringing this Newsletter in time. I sincerely thank our team who shared their experience, suggested the kind of contents and material in bringing this up.

Lot of interesting and important events are conducted/organized by ComSoc. ***5G Series Workshop*** (not wrong if we call it our flagship event) is getting a wide popularity. My sincere thanks and request to all the members to make it further better.

I would also like to sincerely thank Bangalore section chair and other office bearers for extending their full support and cooperation to ComSoc chapter. Similarly, hearty thank to IEEE staff especially Munir Mohammed who has been always with us.

I might have missed some event or some major initiative from some IEEE Volunteers in this message, albeit inadvertently. Please bring the major efforts to my notice so that those can be highlighted in the later editions.

I am sure that with the help of active IEEE volunteers, we will be able to keep the momentum in publishing attractive IEEE ComSoc-BIN in the months and years to come, which will be of archival value.

With warm regards,

Navin Kumar, PhD
Chairman, IEEE ComSoc Bangalore Chapter
navinkumar@ieee.org

About IEEE ComSoc and ComSoc Bangalore Chapter

Since IEEE Communications Society (ComSoc) began operations in January 1972 (IEEE founded in 1963) as an independent Society of The Institute of Electrical and Electronics Engineers (IEEE) with over 32,000 members, IEEE ComSoc has become the premier international forum for the exchange of ideas on communications technologies and information networking.

IEEE ComSoc has evolved into a diverse group of global industry professionals with a common interest in advancing all communications technologies. Members interact across international and technological borders to: Produce publications; Organize conferences; Foster educational programs; Promote local activities; Work on technical committees.

IEEE GLOBECOM, IEEE ICC, and other conferences have earned international reputations. Publications increasingly support local and international coverage of important issues, and the Board of Governors reflects the changing direction of global communications technology.

Volunteer members of the society shape the course of IEEE ComSoc, its publications, technical activities, and conferences while the society's strength comes from the vision and dedication of its members and staff.

IEEE ComSoc members stay on top of the world of communications technology by accessing up-to-the-minute technical information, networking with other experts in the field, and leveraging many other exclusive benefits.

Formed in 2008 by an initiative from Prof T Srinivas, IISc, ComSoc Bangalore chapter has evolved and currently enjoys around 300 professional members from academia and industry. Today, ComSoc Bangalore chapter is one of the most vibrant and dynamic chapters with a large number of expert volunteers performing diverse tasks for the growth of the society and lives of the people. ComSoc Bangalore Chapter is known for the quality event. A huge support is extended to ComSoc chapter and volunteers by industry around.

The current list of volunteers and the important events for the year 2017 is listed below.

Current ComSoc ExCom:

Chair: Navin Kumar, PhD, (Amrita University),

Vice Chair: **Dilip Krishnaswamy**, PhD, (IBM)

Vice Chair**: Shashidhara Dongre**, (L&T Services)

Secretary: **A T Kishore**, (UTL Training Ltd)

Treasurer: **Anand M**, (CDoT)

Member: **Thanmay Menon**, (IISc)

Member: **Reema Sharma**, (Oxford College of Engr)

Member: **Udaya Shankar V**, PhD, (IISc)

Member: **Aloknath De**, PhD, (Samsung)

Member: **Prasad Mantri**, (Semiconductor)

Member: **A.S.Mahadevan**, (IISc)

Member: **A. Paventhan**, PhD (ERNET)

Member: **Jomy Jose**, (L&T Services)

Member: **R.V.Siva Reddy**, PhD (Reva Univ)

Member: **Sambit Kumar Patra**, PhD

Member: **Prakash R**, (CDoT)

Member: **Radhakrishna A**, (thingTronics Innovation)

Member: **Sudhir.K.Routray**, PhD, (CMRIT)

Member: **Krupa Rasane**, PhD, (VTU Belagavi)

Member: **Syam Madanapalli**, (Dell)

Student Rep: **Ms Sindhu.V**, (GITAM)

Student Rep: **Ms S.Shaambhavi Shrivastava**, (Amrita Univ)

Immediate Past Chair**: B N Pal, (Shristi ESDM Pvt Ltd)**

CHAIR Bangalore Section**: Prof Debabrata Das, (IIITB)**

Important Events:

Event Name	Date and Month	Venue
Global 5g Tutorial Series	Jan, 19, 2017	Taj Vivanta, M G Road
Workshop on Advances in 5G and HetNet	Mar, 20, 2017	IISc, Bangalore
Insights into Cloud Security and Creating & Managing Cloud Networks	Apr, 29, 2017	Avaya India Pvt Ltd, AMR Tech Park Bommanhalli
Workshop in Research Methodology	May 8-9, 2017	CMRIT, ITPL Road
Smart City Knowledge Workshop Series	May 26-27, 2017:	Belagavi (Belgaun)
Open Challenge for Working Model/Project focused on Smart City/IoT by UG/PG Students	Jun 30, 2017	Bangalore (yet to finalize)
Two Days Research Methodology (main focus on Paper Writing and Research)	Jul 9-10, 2017	Amrita School of Engineering *
5G Technology Challenges and Open Issues	Aug 21, 2017	Mysore SJCE
Intelligent Transportation Systems: How to improve Raod traffic in Bangalore	Sep 2017	Bangalore
5G Internet of Things One day workshop	Oct 2017	TBA
Placeholder for possible four smart city events TBd	TBD	TBD

5G WORKSHOP SERIES: AN INITIATIVE BY COMSOC CHAPTER

IEEE ComSoc Chapter Bangalore (India) has been one of the very dynamic chapters. Being very rich city in technology (the second Silicon Valley), the ComSoc Chapter enjoys experienced and technology expert volunteers. The ExCom members in 2014 initiated conducting workshop series in advanced communication specifically on 5G Cellular Systems when the entire world started talking and investigating about this. The first workshop conducted on "***Advanced LTE and Beyond"*** on 13-14 Sep 2014 led by Dr Navin Kumar, an ExCom member. The workshop was addressed by 9 speakers from academia and industry like Nokia Inc., L&T Infotech. Samsung, etc. While the industry experts focused more on development of LTE-A the speakers from academia like Prof Neelesh and Navin highlighted and introduced about 5G Cellular Technology. The workshop conducted @ Indian Institute of Science (IISc), Bangalore was attended by over 60 participants mostly from industry and was considered a great success.

Looking at the response and interests from working engineers, scholars and faculties; the chapter set an agenda and planned to conduct at least two events every year to generate interests among engineers and researchers to enable global competency in the development of 5G Cellular. The main focus of this organizing team ComSoc Bangalore Chapter was set to 5G Technology development, current trend and research challenges. The ExCom planned to conduct series of events on this area which was widely accepted and supported by industry and participants. The aim of the workshop series is to spread the awareness of 5G Cellular Development and participation/contribution in the research from India. This series of workshop is apart from various others activities like Software Defined Networks (SDN), Smart City, Research Methodology etc, that ComSoc chapter periodically organizes.

The next edition (2nd) of the "***5G Wireless Technologies***" workshop series organized on 22-23 May, 2015 at Capital Hotel, Bangalore with over 85 participations. This workshop discussed in detail starting from introduction of 5G Technology to testing and measurement challenges towards 5G development. This workshop attracted speakers from Huawei, Tejas Networks, Nokia, CDoT, Qualcomm, Samsung, Keysight, TCS, Rohde & Schwarz including Professor from Indian Institute of Technology. They discussed various technology options from Physical layer to application layers or the use cases including specific to Indian scenario. Almost all necessary and prospective technologies were discussed in the workshop. The workshop also included a panel session on "5G in India: the Challenges and Opportunities" moderated by Dr Navin from Amrita University and panellist were from Lekha Wireless, Nokia, Samsung, Alcatel Lucent and UTL Technology. The workshop was very interacting and considered a very great success.

The visibility and popularity started growing and more participation and interest seen from the industry representatives. Nokia Inc. came forward to host the next edition of the workshop and extended their facilities in Manayata Embassy Tech Park, Bangalore. Manayata Tech Park houses over 100 companies including most of the MNCs. The outcome of the discussion led to one day workshop on "**5G Technology Enabler: Use Cases"** on 12th December, 2015. The workshop speakers were from Qualcomm, NanoCell, Keysight, CDoT and Dr Navin himself. Over 100 participants attended the events which included around 40 from Nokia employees. The workshop ended with a panel discussion. This was another great event on 5G related technologies.

Thus, the event on 5G has become a trademark of Bangalore ComSoc chapter and conducts at least two events annually either 3 days or 4 days. In 2017, one day tutorial from IEEE 5G Initiative took place on 9th January where Dr Ashutosh Dutta, the technical director IEEE 5G Initiative, Dr Sudhir Dixit and many other prominent speakers spoke at various verticals of the 5G. The latest, the 7th in series, "**Advances in 5G Networks and HetNet**" organized on 20th March, 2017, was conducted at Indian Institute of Science Bangalore with the theme on Small Cell and HetNet by merging a DL by Dr Ashutosh Dutta, a guest speaker Prof. Lajos Hanjo from University of Southampton UK and other speakers from Aricent, Samsung, Tieto Inc, QuadGen Wireless, etc. Over 100 working engineers and research scholars attended the workshop. The Bangalore section Chair, Debabrata Das, Secretary, Mr B N Pal, immediate past chair Prof. Hari along with many members from section and chapter participated in the workshop. Various aspects of 5G like Physical Layer in details including challenges for both narrow band and wide band on different frequency bands such as 6-sub GHz and millimetre Wave (mmWave) were discussed. Speaker from Samsung discussed the ongoing development at Samsung, prototype testing and evaluation in Korea, current status both on mmWave and sub GHz band. Prof Lajos gave a brief idea, role and necessity of heterogeneous networks. He also threw many challenges and some of the solutions. Dr Ashutosh, a security specialist discussed the important solutions in security and challenges ahead. He also demonstrated some of the product solution that his team developed in the company. Similarly, there was a very interactive session on machine-to-machine communication and small cell based networks. The workshop was very interactive and participants were very happy to interact with experts in the workshop. The final brief session was an introduction to IEEE ComSoc, its 5G Initiative and invitation to join the research group and contribute to 5G developments. Some of the photos of the event are enclosed.

We would like to continue this workshop to ensure participation, engagement from industry and motivation of people to contribute to 5G development and standards. We also plan to take the workshop in nearby city and areas. We have already started doing this but not on 5G. In fact, ComSoc Bangalore has got 'quality' as feedback from people around.

Please look at the upcoming events or keep track of the following link for the next workshop.

More information is provided at: http://bangalore.chapters.comsoc.org/events-3/

FIG: 5G EVENT SNAP

VEDIC MATHEMATICS FOR HIGH SPEED DATA SECURITY IN WIRELESS COMMUNICATION

Dr. Abdul Kareem
Principal, Bearys Institute of Technology, Mangalore

Security is one of the fundamental requirements in wireless communication. With the advent in wireless technology, there is always a need for high speed data security. Security in communication is provided by means of cryptographic algorithms. Among the available cryptographic algorithms, Rivest-Shamir-Adleman (RSA_ algorithm is the most widely used asymmetric key algorithm. Many protocols, such as SSH, SSL/TLS employ RSA are used. The high speed operation of algorithm is very essential for systems operating at high frequency. The computational overheads in the algorithm may affect the speed of operation and hence there is always a need of high speed computation. The execution speed of RSA algorithm can be increased by employing concepts of Vedic Mathematics to reduce the computational time and hence making the algorithm work faster. Vedic Mathematics provides sixteen sutras which deals with various mathematical operations. These sutras can save a significant amount of computational time, by eliminating unnecessary steps involved in the conventional computation. Application of these Vedic sutras in RSA algorithm greatly increases the speed of execution. RSA algorithm involves the multiplication of large primes, for the computation of the private and public keys. The computational time can be greatly reduced by employing the Vedic sutra Urdhva Tiryagbhyam, instead of conventional computation. Vedic sutra Nikhilam and Paravartya-Yojayet can be used for the computation of mod value, which is faster as compared with the existing algorithms. With the help of Vedic techniques, for high speed data security can be achieved. Various other cryptographic algorithms are also used in WLAN technology based on IEEE 802.11, Wi-Fi and other standards. Elliptic curve cryptography (ECC) is another widely used cryptographic algorithm which uses algebraic structure of elliptic curves over finite fields. Vedic Sutras can also be applied for ECC to solve the curves efficiently. Vedic Mathematics provides a wide variety of sutras which solve the given problem in efficient way. Exploiting this attribute of ancient Vedic techniques and application of it can enhance the speed of cryptographic algorithms in wireless communication.

IMPORTANT LINKS

http://www.comsoc.org/
http://www.comsoc.org/whitepapers
http://www.comsoc.org/tech-focus
http://icc2017.ieee-icc.org/
http://www.comsoc.org/comstandardsmag
http://globalpolicy.ieee.org/wp-content/uploads/2017/02/IEEE17001.pdf
http://www.ieee.org/about/volunteers/volunteer_index.html?WT.mc_id=dhtml_vol_see
http://www.comsoc.org/free-tutorials
http://www.comsoc.org/training/training-calendar/road-5g
http://www.comsoc.org/ctn/death-and-possible-rebirth-dsp

PROVENANCE OF DIGITAL ASSETS -BLOCK CHAINS AND BIT MARKS

Asha Joseph, Member, IEEE, Associate Professor, Bangalore Technological Institute, Bangalore

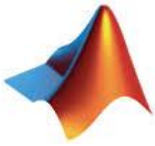
The concept of blockchain belongs to Satoshi Nakamoto (2008) and as a core component of the digital currency bitcoin, where it serves as the public ledger for all transactions. A blockchain is a distributed database that maintains a growing list of records called blocks. Each block contains a timestamp and a link to a previous block. Once recorded, the data in a block cannot be altered. A peer-to-peer network and a distributed time stamping server is commonly deployed for a blockchain and is managed autonomously. Thus, blockchains are open, distributed ledger that can record transactions between two parties efficiently and in a verifiable and permanent way.

This concept is used to implement a system where digital assets ownership and transfer of ownership is safely recorded and maintained in a distributed database called Bitmarks. Every digital entity can be represented by a unique identifying characteristic, or "fingerprint" using a cryptographic hash function. Every person who is involved in the ownership and transfer will have a unique digital certificate to identify them.

Given the unique identifier of the digital asset, a chain of ownership, called ”provenance”, is recorded in a blockchain. Such a "title" to a digital asset is called a Bitmark. Bitmark transfers are peer-to-peer, publicly verifiable, unforgeable and fully compatible with existing property law. In other words, Bitmark keeps and tracks information about the ownership and transfers of ownership/provenance of any digital asset. When cybercrimes like digital property theft happens, this provenance information maintained by Bitmark system can be readily used to track the original owner and current owner of the digital asset.

Any new asset can be brought into bitmark system by creating an asset record and a bitmark with an issue record (no transfer record initially) for it in the bitmark system server named bitmarkd (bitmark daemon). This is done by making use of JSON RPC interfaces of bitmarkd. The prerequisites of public key (Ed25519) and other cryptographic keys on client side are assumed to be standard PKI concepts. Bitmark system is a very recent and upcoming technology (https://bitmark.com) and has potential to provide supporting data for solving one of the prominent digital crimes - i.e. digital property theft. This method is particularly suitable for digital multimedia assets like photos and videos.

SIMULATE 3GPP 5G NEW RADIO TECHNOLOGIES

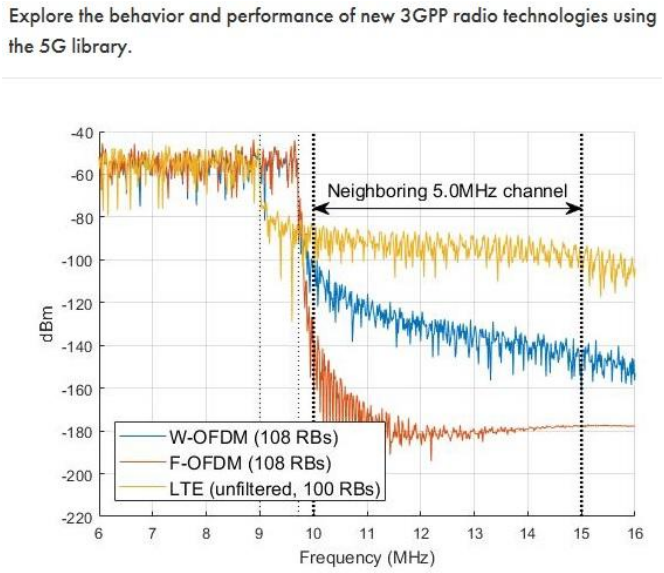


MathWorks®

The **5G library** is a free, downloadable add-on for the **LTE System Toolbox** in MATLAB. It provides functions and link-level reference designs that allow you to explore the behavior and performance of new 3GPP radio technologies.

The library allows you to simulate the following:

- Channel models, including tapped delay line (TDL) and clustered delay line (CDL) channel models as specified in 3GPP TR 38.900.
- New radio waveforms, including candidate algorithms to improve spectral efficiency by limiting out-of-band emissions. These algorithms include:
  - ✓ Filtered OFDM (F-OFDM)
  - ✓ Windowed OFDM (W-OFDM)
  - ✓ Cyclic Prefix OFDM (CP-OFDM)
- Link-level simulation reference design, enabling you to measure the throughput of a 5G link using the provided waveforms and channel models.



https://in.mathworks.com/products/lte-system/features.html?s_tid=srchtitle#5g-library

Dear Reader, we plan to dedicate this page for 5G Tutorial Series. Starting from the basic, I would like to continue discussing about 5G Cellular System and Technologies in sequence (starting from Part 1, Part 2, ...The tutorial will be in continuation from the previous issue. I hope, we will go in parallel with ongoing 5G research and development. It is believed that the reader will gain better understanding of 5G Cellular System if they follow the tutorial. In this Part 1, we start with the basic definition, important specifications. Some of the questions like, what is 5G, why is the 5G and when is the 5G are expected to be answered in this issue. I would welcome any suggestion from you.

Navin Kumar, PhD, Associate Professor, Amrita School of Engineering Bangalore

5G Technology and Cellular System Tutorial Series: Part 1 – Introduction To 5G Including Expected Specifications

Fifth Generation (5G) mobile communication is the proposed next generation of cellular standards beyond currently used 4G/IMT Advanced such as long term evolution–advanced (LTE-A). A new mobile generation has appeared approximately every 10 years since the first 1G system introduced in 1982 (unfortunately, in India it was not used). The first '2G' system (such as GSM standard) was commercially deployed in 1992, and the 3G system (UMTS) appeared in 2001. 4G systems fully compliant with IMT Advanced were first standardized in 2012. It is expected that the early release of 5G system would be in 2020.

New mobile generations are typically assigned new frequency bands and wider spectral bandwidth per frequency channel (1G up to 30KHz, 2G up to 200KHz, 3G up to 5MHz and 4G up to 20MHz. 5G is expected to have much higher bandwidth as far as data rate is concerned. In addition, much technological advancement such as overall architecture, technologies at different layers. is made from 2G to 4G. Previous generations like 3G were considered a breakthrough in communications. 3G receives a signal from the nearest phone tower and is used for phone calls, messaging and data. 4G works the same as 3G but with a faster Internet connection and a lower latency (the time between cause and effect). 4G claims to be around five times faster than existing 3G services and theoretically it can provide download speeds of up to 100Mbps. 5G is expected to be of much higher speed (greater than 1Gbps) than 4G cellular.

One of the main drivers for the 5G cellular mobile system is the data demand specifically mobile data and to meet the higher data rate (bit per second), the wider channel is normally required. Though, there are other methods like multiple input and multiple output (MIMO) to increase the channel capacity but the cost and complexity becomes much higher.

5G Wi-Fi wireless local area network (WLAN) connections are set to be about three times faster than 4G cellular, starting with 450Mbps in single-stream, 900Mbps (dual- stream) and 1.3G bps (three-stream).

5G cellular will be significantly faster than 4G, allowing for higher productivity across all capable devices with a theoretical download speed of 10,000Mbps. Plus, with greater bandwidth come faster download speeds and the ability to run more complex mobile Internet applications.

One other important driver for the 5G cellular system is the massive connectivity. We are already starting to see a huge growth in Internet of Things (IoT) and smart devices, 5G's speed and capacity will enable an even more rapid arrival of this connected future.

5G offers enormous potential for both consumers and industry. 5G holds the promise of applications with high social and economic value, leading to a 'hyper-connected society' in which mobile will play an ever more important role in people's lives. Discussion around 5G falls broadly into two schools of thought: a service-led view which sees 5G as a consolidation of 2G, 3G, 4G, Wi-Fi and other innovations providing far greater coverage and always-on reliability; and a second view driven by a step change in data speed and order of magnitude reduction in end-to-end latency.

Any new 5th generation, 5G cellular technology needs to provide significant gains over previous systems to provide an adequate business case for mobile operators to invest in any new system. Facilities that might be seen with 5G technology include far better levels of connectivity and coverage. For 5G technology to be able to achieve this, new methods of connecting will be required. Looking back on existing system, the main drawbacks with previous generations is lack of coverage, dropped calls and low performance at cell edges. 5G technology will need to address this.

5G Specifications

Although, the standards bodies have not yet defined the parameters needed to meet a 5G performance level, other research and development organisations have set their own aims that may eventually influence the final specifications. In summary, Fig.1 and Fig.2 describe the some of the requirements and expectations from 5G cellular system. Figures are self explanatory and easily readable.

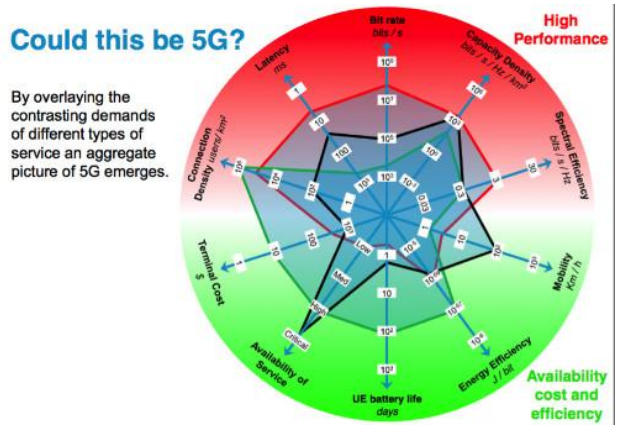


Fig.1:Expected specifications for no. of performance parameters

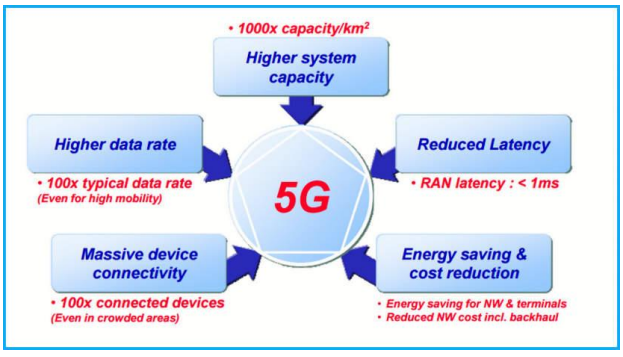


Fig.2: High Level Expectation from 5G

To be continued in Part 2 (Aug 2017 Issue of ComSoc-BIN)....

ENHANCING PITCH DETECTION ACCURACY USING FOURIER SERIES APPROXIMATION

- *Balachandra Kumaraswamy, P. G. Poonacha*
International Institute of Information Technology, Bangalore

Pitch detection forms one of the primary areas of research in the field of Music Information Retrieval (MIR). Pitch can be defined as perception of fundamental frequency f_0 of the signal. By mathematics, fundamental frequency is given as inverse of the fundamental period T of the signal. Hence most pitch detection algorithms are designed to find either T or f_0 of the signal. Various pitch detection algorithms have been proposed over the past few decades with an assumption that the given signal is perfectly periodic. When these algorithms are applied on quasi-periodic signals, the performance starts to deteriorate. One of the prominent errors occurring across all pitch detection algorithms is "harmonic error". Here the estimated pitch is one of the multiples of the actual pitch of the signal. In other words, a multiple of T or f_0 is estimated as the period or frequency of the signal. We apply and analyze some of the popular pitch detection algorithms viz., Auto-Correlation function (ACF), Square Difference Function (SDF), Average Magnitude Difference Function (AMDF), Cepstrum and Harmonic Product Spectrum (HPS) to harmonic signals to understand the cause of such harmonic errors. We then have proposed a pitch detection algorithm using Fourier series to enhance the accuracy of pitch estimation by identifying the fundamental frequency of the signal. Fourier series Approximation Method (FAM) gives a periodic approximation of the quasi-periodic music signals and thus helps in understanding the nature of the signals by analyzing the strength of harmonics of the signal. This helps us to get to the root of the problem resulting in harmonic errors and in correcting the same.

Since a periodic signal satisfies the equation x(t) = x(t + nT) for any integer n, there is an inherent problem of estimating the fundamental period as a multiple of T for all pitch detection algorithms. A signal which has strong even and weak odd harmonics can result in estimating the fundamental frequency as double the actual f_0(or T/2 as period). Similarly, signal with strong harmonics at multiples of 3 and 4 can result in estimation of pitch as $3f_0$ or $4f_0$ respectively.

Pitch detection is applied for signals by breaking into small chunks with the help of windowing function of length W. Fourier series approximation for a windowed signal using time period τ can be obtained using the equation $\tilde{x}(t) = a_0 + \sum_{k=1}^{N} a_k \cos(2\pi kt/\tau) + \sum_{k=1}^{N} b_k \sin(2\pi kt/\tau)$. All the popular pitch detection algorithms mentioned are applied first on the given windowed signal then the initial estimate of $\tau(\tau_{guess})$ is taken by considering the time period which is given by maximum number of algorithms. Our aim here is to find the correct octave or harmonic of the fundamental and hence the assumption that the initial estimate of the time period is one of the multiples of the actual T is made. In this work, we focus only on fixing the harmonic errors.

Then vector forming the multiples of τ_{guess} is formed which is of the form (…,τ_{guess}/4, τ_{guess}/3, τ_{guess}/2,τ_{guess} , 2τ_{guess} , 3τ_{guess} , 4τ_{guess} ,…). The Fourier approximation is obtained for each of the values of τin τ_{guess} vector and Minimum Squared Error (MSE) is calculated by taking the difference between the windowed signal and the Fourier approximated signal using the equation $MSE(\tau) = \sum_{j=1}^{W} (x(j) - \tilde{x}(j)|_\tau)^2$ where $\tilde{x}(j)|_\tau$ denotes the Fourier Approximation for a specific value of τ.

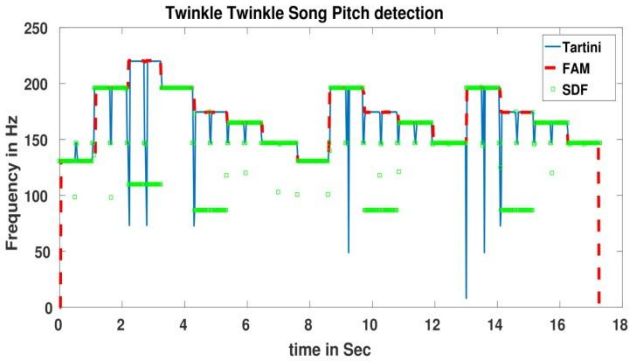


Fig. 1: Comparison of Detected pitch vs time plot for the jingle Twinkle Twinkle Little Star using Fourier approximation, SDF and Tartini

Ideally the best estimation of τ gives the least MSE. But, instead of just finding the τ which gives the global minimum and declaring that as the best estimate of T, we find the global minimum and also find all the local minima which are within a certain threshold of the global minimum. The strength of harmonics w.r.t. all these minima given by coefficients a_k and b_k are calculated using $abVector = (HM)^{-1}X$ where X is the windowed signal of size W and HM which denotes the Harmonics Matrix of size W x (2N + 1) can be obtained using:

$$HM = \begin{bmatrix} 1 & \cos\left(\frac{2\pi}{\tau}(1:N)(1)\right) & \sin\left(\frac{2\pi}{\tau}(1:N)(1)\right) \\ 1 & \cos\left(\frac{2\pi}{\tau}(1:N)(2)\right) & \sin\left(\frac{2\pi}{\tau}(1:N)(2)\right) \\ : & & : \\ : & Wrows & : \\ : & & : \\ 1 & \cos\left(\frac{2\pi}{\tau}(1:N)(W)\right) & \sin\left(\frac{2\pi}{\tau}(1:N)(W)\right) \end{bmatrix}$$

Since HM is not a square matrix we find the pseudo-inverse of the matrix using Singular Value Decomposition. Once 2N + 1 coefficients are obtained we find the Fourier approximation for τ samples and repeat the same approximation to cover the entire length W of the window. Then MSE is calculated. We compare the Fourier coefficients obtained for different values of τ corresponding to minima. We find the number of strong harmonics and weak harmonics for each of the τ and then arrive at the best estimate of the time period.

For e.g. a signal with strong even harmonics can lead to estimation of time period as T/2 (τ_{guess}) (i.e. $2f_0$) in place of *T*. When we find the Fourier approximation (FA) and compare the coefficients obtained for time periods *T* and *T/2*, we observe that odd Fourier coefficients are weak and even coefficients are strong w.r.t. *T*. The harmonics present at 2, 4, 6, 8, w.r.t. *T* are present at 1, 3, 5, 7, when FA is obtained with T/2 as period. If the number of weak odd harmonics are above a certain threshold as compared to number of strong even harmonics in the case of FA with *T*, we conclude that $2\tau_{guess}$ is the best estimate else τ_{guess} is the best estimate of the time period. Similarly, for different harmonic signals by comparing the number of weak and strong harmonics for various multiples of τ_{guess} the structure of the actual signal can be understood and a better estimation of the pitch can be obtained. An example of how the octave correction can be done using FAM is shown in Figure 1. Here the detected pitches are compared with a pitch detection software Tartini and SDF method.

HARDWARE-IN-LOOP SIMULATION FOR SUPER WIFI

Suma M N, Associate Professor BMS College of Engineering

TV White spaces are resources that capitalise on the government's long-term goal of total Internet penetration in our country. It is possible to reach 800 million offline citizens and bring them into the Internet ecosystem, which would facilitate a transformational impact on the country's social, economic and political landscape.

One such method is to employ super WiFi. The IEEE 802.11af framework, referred to as 'White-Fi' or 'Super WiFi' is a wireless computer networking standard in the IEEE 802.11 family that allows WLAN operation in the TV White Space spectrum in the VHF and UHF bands in between 54 and 790MHz (USA), 470-790MHz (Europe) and 470-698MHz (India).

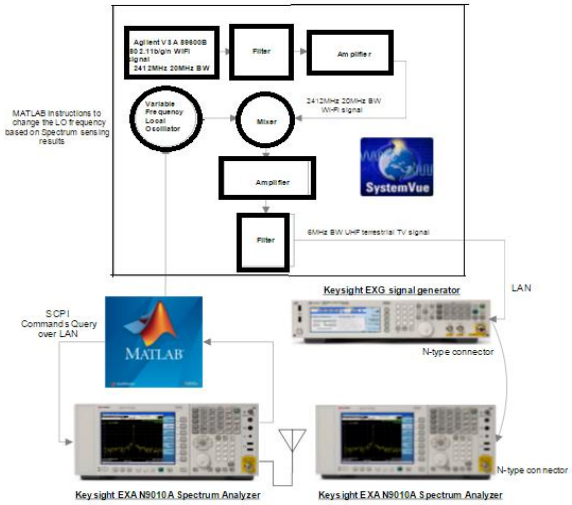


Figure: Hardware-in-loop Simulation Setup

This standard was approved in 2014 and various cognitive radio technologies to facilitate the efficient use of these unused TV channels while limiting interference for primary users are currently being researched.

Hardware-in-Loop simulation to validate our design compliance with IEEE 802.11af specifications can be performed with simple laboratory set up. Hardware-in-Loop processing system employing a consolidated UHF scanner, Network Processor, UHF Translator and the Wi-Fi source is shown in the above figure.

The UHF scanner employed in the prototype is the spectrum analyzer equipped with the whip antenna used to scan the Terrestrial UHF TV spectrum in India ranging from 470-582MHz. The Network Processor in this Hardware-in-Loop system is programmed in MATLAB script that connects to spectrum analyser. Channel power levels are queried by the MATLAB script periodically to detect any activity on these channels.

The 802.11b WiFi signal generated can be from software or through WiFi modules.UHF translator then translates WiFi to UHF band and transmitted through white spaces.

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CALL FOR CONTRIBUTION TO COMSOC-BIN

Please get in touch with us if you wish to write and to be included in this newsletter (in the area of Communication Technology). The article should be from 300-1000 words in docx or doc file and separate image jpeg or tiff file format. You can submit to: (navinkumar@ieee.org)

DEVELOPMENT OF A NANO-DEVICE FOR BIO-MEDICAL ENGINEERING APPLICATIONS

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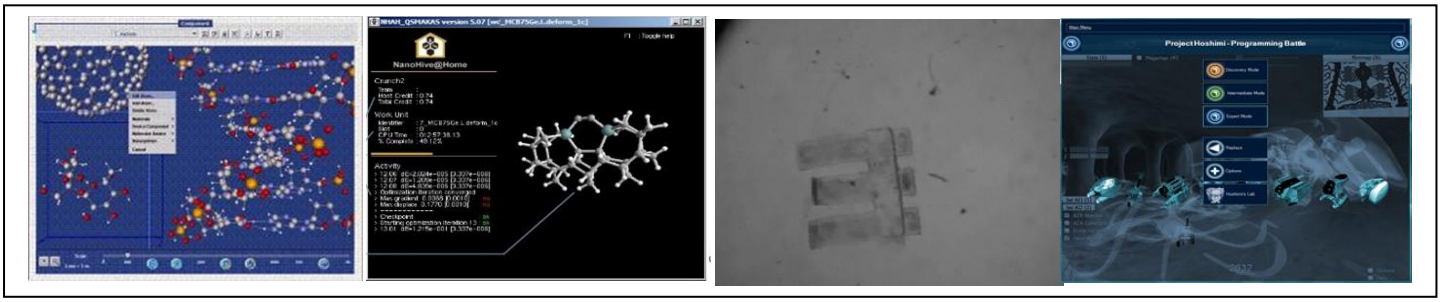
Atoms are the building blocks for all matter in our universe. You and everything around you and us are made up of atoms and molecules. Nature has perfected the science of mfg. matter molecularly. For instance, our bodies are assembled in a specific manner from millions of living cells. Cells are nature's micro/nano machine's. This technique of building devices up to the molecular level is what is called as molecular nano technology and is distinguished by its interdisciplinary nature. With this small background, we have designed a nano-robot from the bio-medical engineering application point of view, i.e., applications w.r.t. biological robots in the field of medicine (bio robotics/bio nanotechnology/molecular nanotechnology) that has been carried out under my supervision. In short, today we have considered the sperm as our ideal model as we have thought that the sperm is the perfect biological delivery system as it generates it's own energy, can traverse rough terrain/fluids and knows how to hone in on its target to deliver the goods. Sperm could be termed out as the most intelligent nano-robot (SNR). While sperm delivers DNA, researchers are now borrowing ideas from sperm to provide energy for nano scale robots aiming to deliver medication from nano-sized medical devices. A funded project "simulation, design and development of nanobot using sophisticated simulation tools-nano hive (undertaken by me as a consultation project w.r.t. the industry-institute interaction)" is stressed upon in this context, starting with the mathematical modeling, followed by the constructional features of nanobot, design & development and the manoeuvring of the same in the virtual environments.

The basic constructional features of a NB that we have constructed a nanorobot has a C-nanotube body, a bio-molecular n-motor that propels it & peptide limbs to orient itself, composed of biological elements such as DNA & proteins, genomes & hence, it can be easily removed from the body, it has sensors, molecular sorting rotors, fins & propellers & has <= 6 DOF, has sensory capabilities to detect the target regions, obstacles & C is the principal element comprising the bulk of a medical nanorobot. The motion dynamics of a n-robot in the fluid is assumed to be of a cubic polynomial. The concepts of Quantum mechanics, Fluid dynamics, Hydraulics, Thermal motions, Friction, $R_{e,}$ Fluid flow, VLSI concepts, System behavior, Brownian motions, Control strategy & Theory of elasticity has been considered in the design. The simulation parameter such as Physical Vein/Capillary/Vessel size, Flow rate through vessel, Differing diffusion coefficients, Model, Mathematical chemical based computations, A 3D environment including bloodstream particles, n-robots, and the proteomic signalling was designed in such a way to meet our designed specifications (of course some of the parameters were assumed). The NanoHive-1 simulation tool, which is a modular nanosys-simulator used for modelling the physical world at a nanometer scale has been used for the design. The purpose of the simulator is to act as a tool for the study, design, simulation, experimentation & development of nano & biological entities. The buckling mode-shape has also been predicted using simulations. The result of a simulation is designed to test various distributed computing mechanisms. While just a test, it's still an interesting simulation to watch. The developed system comprises of ~20,000 atoms & runs for 5.5 ps of simulation time. The application of this developed device could in the near future scope in the nano-robots field that could be used for all types of bio medical engineering applications in the mankind.



eFPGAs and the Road Ahead

Raghuraman R Sr Member, IEEE
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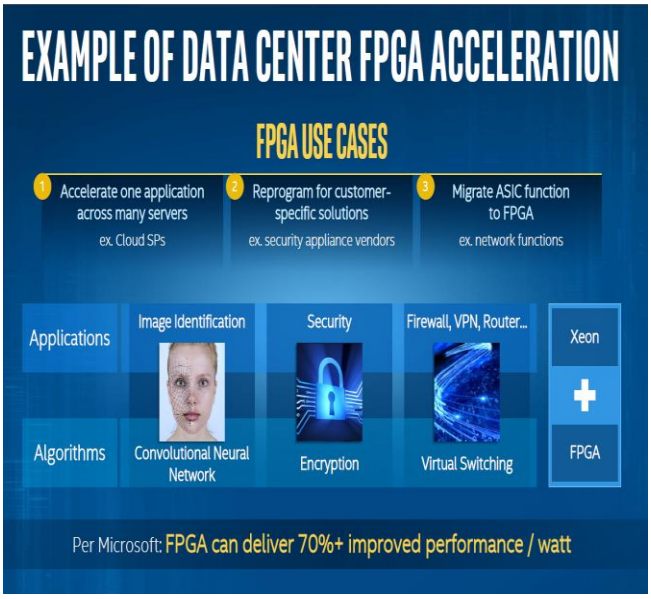
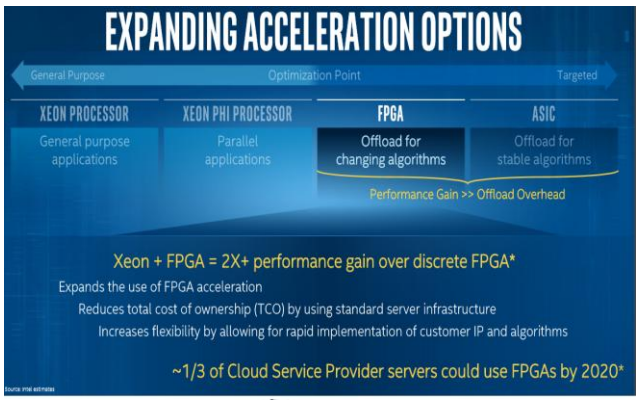
FPGAs are the closest to one-chip-fits-all-applications device. While there are multiple processors ranging from popular CPUs (Central Processing Unit) to GPU (Graphics Processing Unit) to MCU (Micro Controller Unit), each has not replaced the other. While FPGAs have been there for long, Intel's acquisition of Altera has brought it back in focus. Though it has been used and viewed as a prototyping device, FPGA fabric has come a long way from configuring minimal logic to synthesizing a processor core like Intel® Atom™. This has been taken further to integrate FPGA in multi-processor and multi-core servers in data centers (see Figure 1). The range of systems where FPGAs can fit in, span across a wide range - from aerospace to accelerators to contemporary cloud and data centers. Different functional specifications (in the form of RTL) can be synthesized in an FPGA and the FPGA can thus morph into a 'new chip'. Most SoC devices have multiple IPs/components with some 'glue logic' that has been designed using traditional ASIC methodologies. This glue logic has been 'amorphous' with neither predictable nor fixed dimensions. Embedded FPGAs (eFPGA) with predictable dimensions are replacing this and also used to offload software ('algorithms') into hardware. Hardwiring smaller segments of software programs (algorithms) into FPGA through accelerators are increasingly used. These algorithms can be changed/fine-tuned later if required by changing FPGA configuration. Unlike software patches that are dependent on the operating systems and versions, FPGA reconfiguration is independent of the software processes running on the hardware.



An important accessory of an FPGA is the software that enables its (re-)configuration to perform the desired functionality in tune with the IPs around it or the SoC in which it is embedded. This software while being native to the FPGA design extends its relevance and importance to eFPGA as well. Embedded FPGA in short is a 'stripped' down version of an FPGA SoC with the IPs around it determined by the actual SoC it is going to reside in and not pre-determined, like the conventional FPGA SoC. Achronix, Flex Logix, QuickLogic are the few companies that have announced eFPGA products with Achronix having a shipping version already along with its ACE™ software. With cloud computing touted to be the next big thing and storage in the cloud already in vogue, the importance of eFPGAs and their usage in servers and compute cannot be understated.



All in Three: How to Pitch Your PhD in 180 Seconds

http://blogs.nature.com/naturejobs/2017/04/24/all-in-three-how-to-pitch-your-phd-in-180-seconds/?WT.mc_id=EMX_NJOBS_0427_NATUREJOBSNEWSLETTER_A&WT.ec_id=EXTERNAL

STUDENT BRANCH CHAPTER INFORMATION

AMRITA SCHOOL OF ENGINEERING, BANGALORE CAMPUS

ASE ComSoc Student Branch Chapter is formed in April 2016. Dr Navin Kumar led from the front to start and reactivate Student Branch ASE. The chapter inaugurated function was scheduled with half day event on 100th Birth Celebration of the Father of Communication Engineering, Shannon Claudio. On this occasion, few guest lectures were organized and a competition was held under the theme of **Portray Shannon's Life and Win Prizes**.

Many events were conducted from that time. This year, the ComSoc Chapter conducted one day workshop on Wireless Sensor Networks and Internet of Things (WSN IoT) on 31 Jan, 2017. On 28th April, an event called "PRADARSHAN" was organized where over 50 groups from over 70 colleges submitted and demonstrated the project hardware/software design. 5-best projects were awarded momentous and cash prize of over 25,000 INR. Over 300 students from different parts witnessed the events.

BATTLE OF PROJECT

@ Amrita School of Engineering,
Submission Open Until 31 May, 2017
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INDIAN INSTITUTE OF SCIENCE

Faculty Advisor – Prof T Srinivas, ECE Dept

RVCE STUDENT BRANCH CHAPTER

RVCE ComSoc Student Branch Chapter is formed in the month of July 2016 with faculty advisor as Dr S Ravishankar, Professor in the Dept. of ECE.

Faculty Coordinator: K S Shushrutha Asst. Professor, Dept. of ECE, RVCE
Student Chair: Prakhar Jain, Student, Dept. of ECE, RVCE

INTERNSHIP/JOB OPPORTUNITIES

Internship opportunity available @ Amrita School of Engineering, Amrita Vishwa Vidyapeetham, Bangalore Campus for both M Tech and B Tech. Contact: Dr Navin (navinkumar@ieee.org) for exploring it. Area – ECE, Photonics, Computer, IoT, LiFi (VLC), ITS, etc.
(note – Amrita University has been TOP Private University in India for last 3 years)
INTERNSHIP for a minimum of 6 months and 3 months AND Job available with Start Up in IoT related work at thingTronics Innovation Pvt Ltd and many others. Contact Dr Navin to get in contact with them.
http://www.thingtronics.com/
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- networking testbeds (both for smart city and for 5G)
Please contact: Dr Navin Kumar (navinkumar@ieee.org)

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THANK YOU NOTE FOR THE CONTRIBUTORS

We would like to thank every author who showed interest and submitted their works. We could not include all of them mainly because of scope and relevance.

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